

Litho-Clean-By-Construction Nanometer Design

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Abstract

The increased complexity of resolution enhancement technology (RET) at nanometer processes is significantly impacting lithographic yield. The major contributors to declining yields are smaller lithographic process window, increased sensitivity to layout topology in the lithographic process, and complex mask rule constraints that impact the application of RET. These issues must be addressed with a fast, accurate and easy to use RET design and verification solutions that detect yield-limiting conditions. Nanometer manufacturability impacts physical design through complex layout rules and large guard-bands for process variability; this creates new requirements for new manufacturing-aware physical design technologies. In this paper we review physical design methodology changes that arise from sub-wavelength lithography and nanometer manufacturing. We will also discuss how foundries are approaching IC designers with pre-checks solutions in order to assure lithography compliance. We will observe new processes effects on physical design methodologies and the EDA on-going solutions. The amazing fact is that the semiconductor industry is still able to use deep ultraviolet (DUV) light for at least the next two to three technology nodes. The industry's move to 193 nm light into the 45 and 32nm technology nodes, however, creates a new arena of optical extension. Process like 45nm means printing features at $\lambda/4$, and 32nm means printing even at $\lambda/6$. The fact is that the industry is already looking into $\lambda/8$. (Figure #1, 2)

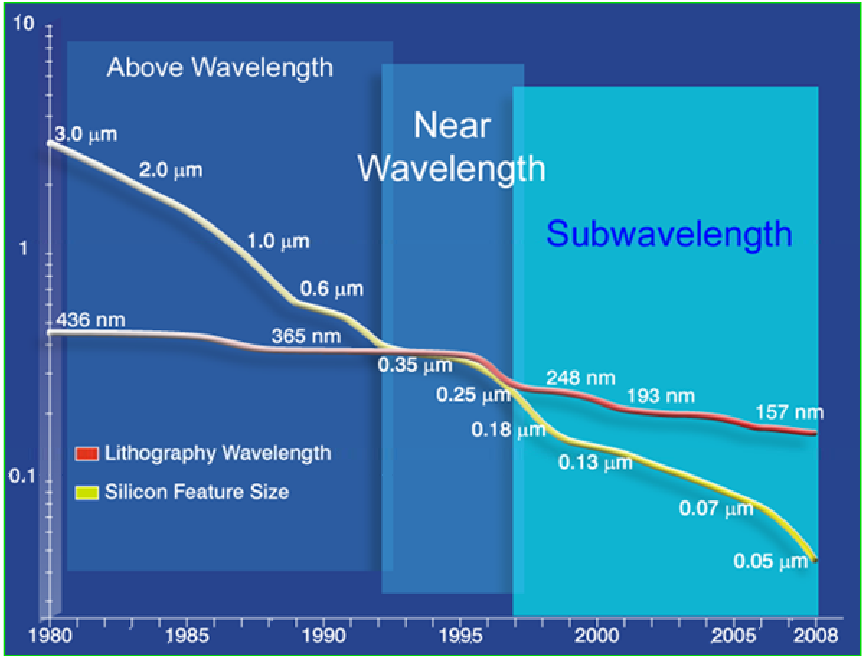


Figure 1: The Sub wavelength gap
Image Source: Numerical Technologies

Introduction

Resolution enhancement technologies (RET) like optical proximity correction (OPC) and phase shift masking (PSM) have significantly increased the cost and complexity of sub-micron nanometer photomasks. The photomask layout is no longer an exact replica of the design layout. As a result, reliably verifying RET synthesis accuracy, structural integrity, and conformance to mask fabrication rules are crucial for the manufacture of nanometer regime VLSI designs. New EDA systems were recently developed consists of efficient wafer-patterning simulators that is able to solve the process physical equations for optical imaging, resist development and hence can achieve high degree accuracy required by mask verification tasks. These tools are able to efficiently evaluate mask performance by simulating edge displacement errors between wafer image and the intended layout. Moore's law continues to drive higher performance with smaller circuit features. Aggressive technology scaling has introduced new variation sources and made process variation control more difficult. As a result, semiconductor manufacturing equipment will be strained to maintain constant process variation levels in future technology nodes. Despite the relaxation of some tolerances, there are no known solutions for a number of near-term variability control requirements according to the ITRS. Consistent improvements in the resolution of optical lithography techniques have been a key enabler of the continuation of Moore's law. However, as minimum feature sizes continue to shrink, the wavelength of light used in modern lithography systems is no longer several times larger than the minimum line dimensions to be printed. As a result, modern CMOS processes are operating in a sub-wavelength lithography regime.

Increasingly complex design rules impact detailed routing, physical verification, resolution enhancement (RET) and mask data preparation. (MDP) The loss in design tool quality as well as design productivity have resulted in increased project uncertainty and manufacturing NRE.

COMPLEXITY BUILDUP IN 90/65/45 nm NODE

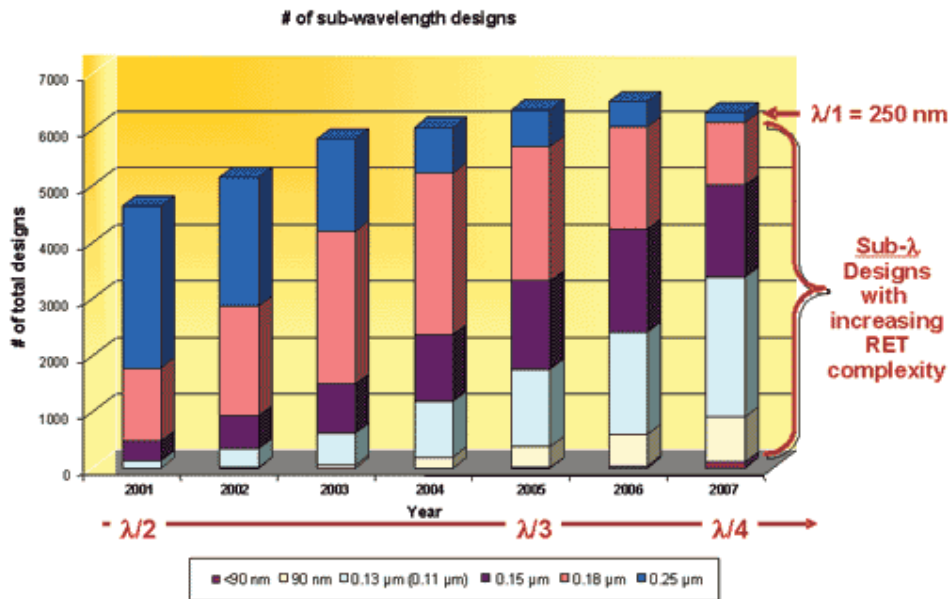


Figure 2: Complexity build-up in 90, 65 and 45 nm nodes
Image Source: IBS

The Lithography Process

The complexities in mask data and manufacturing make it highly desirable to verify and optimize the mask data independently before committing to the costly fabrication process. An effective method for post-RET mask data verification is to simulate its image on the silicon wafer and compare it with the original design intent. This method places mask data in its intended operating environment and evaluate its performance metrics that have direct impact on wafer imaging. A simulation based verification system can evaluate the process for a product and give warning on certain performance limiting spots on the layout and thus significantly reduce the risk of mask data errors.

Once the troubling spots are identified, localized corrections can be applied to extend the process window in an intelligent way. The existing model based mask layout verification systems have a few areas that require further improvement. First, they are typically implemented with the same simulation engine with model based OPC. Sharing the simulation engine with OPC, the verification also inherits the errors of the OPC model. The logical dependency jeopardizes the probability of finding OPC errors, and reduces the reliability of the verification. A process window is the range of process parameter variations under which the line width remains within limits. Secondly; they employ empirical modeling approaches that cannot easily track acceptable variations in process conditions.

In order to sample a different condition in the process window, a different set of models has to be developed, which consumes significant effort and time. In addition, there is no inherent reason why one set empirical models can judge the result of another if they are derived from the same set of mathematical formulation and training patterns. A full-featured photolithography simulator for mask data verification has been developed for the past decade by the major EDA vendors. (Mentor Graphics, Cadence) These types of simulators have been used extensively in lithography process development where they have demonstrated high accuracy for process predictions.

A mask data verification flow around the physical lithography simulation core that is independent from the OPC engine, thus free from the logical dependency between OPC and its verification. The use of physical models opens the possibility for achieving higher prediction accuracy on complex layout configurations. In addition, physical model can naturally predict the pattern transfer behavior under process variations such as focus change. Furthermore, a physical layout design can efficiently leverage this physical model simulator to improve circuit performance and reduce the manufacturing variations. The lithography process is highly dependent on mask-making capabilities. The common process are binary, etch quartz, single/double/multiple exposure. At 180 nm few users moved toward alternating PSM. (Phase Shift Mask) Etched quartz masks have not been accepted in the IC's market despite their apparent resolution and process window enhancement capabilities.

AltPSM first appearance was as an unmanageable triple phase step, resulting in four levels of mask writing procedure. Then it was replaced by a dual-exposure step as a complementary PSM (cPSM). The main issue with double exposure is its high cost for manufacturing. This is a direct result of most advanced and costly manufacturing systems. Another option which is still under evaluation is the Chrome-less Phase Lithography (CPL), an etched quartz mask that should have the advantages of PSM although is done in a single exposure. (Figure #3) Historically, lithography has taken the most conservative path which is binary image masks (BIMs), which seems to be the safest course. Recent improvements are involved double exposure which basically is pushing the boundary of optical extension. The industry is constantly evaluating other types of lithography processes in a continue effort to provide an effective yet affordable solutions.

CPL-PSM vs. altPSM

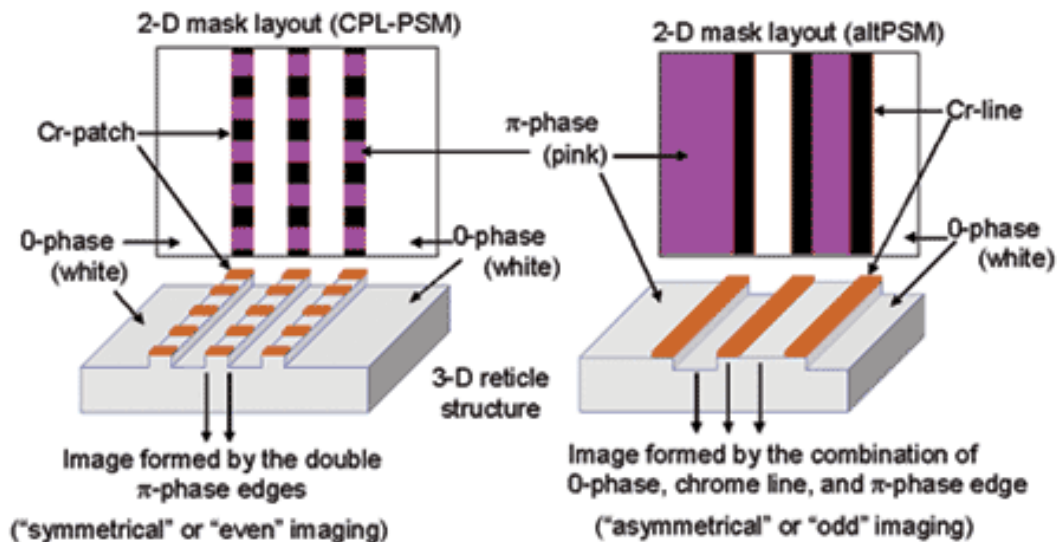


Figure 3: CPL-PSM with Chrome patch comparing to altPSM.
Image Source: ASML MaskTools

Lithography's Impact on Physical Design

Optical lithography is being pushed to new extremes especially with the move to 45 & 32nm processes. The extension of optical lithography has been enabled by several developments such as chemically amplified photoresists and anti-reflective coatings. By predicting physical phenomena (especially diffraction and interference) behind optical systems and systematically compensating for them, the minimum feature and pitch that can be resolved are significantly extended. These Resolution Enhancement Techniques (RETs) are aimed at three major optical wave components, namely, direction, amplitude and phase. Off Axis Illumination (OAI) techniques direct light at the photomask only at certain angles. The combination of the angle and the pitch of features in the mask can enhance resolution of certain pitches, particularly dense pitches and small lines. The design rules are complicated by the fact that certain large as well as certain fine pitches are well reproduced but some intermediate pitches may not print as well. This leads to some forbidden pitches and sizes.

Optical Proximity Correction (OPC) makes small alterations to the layout features to reduce line-width variation. Sub Resolution Assist Features (SRAFs) or scatter bars are added to the mask to allow isolated features diffract light as dense features but they do not print. Adding SRAFs to intermediate pitches can be tough resulting in suboptimal printing performance for these features. A concern here is that one might be perform double OPC action due to legacy design rules which lead to unnecessary constraints for designers as well as lithographers. The third category, phase, is controlled by Phase Shifting Masks (PSM). Parts of the mask are etched to create phase difference between regions and can enhance resolution for certain features by up to a factor of two. Generating phase-compliant layouts is a major problem for future physical design. An example consequence is the impact on routing algorithms. As we move into deep nanometer regime, some of the requirements such as spacing rules, reliability, signal integrity and process antenna rules impose severe constraints on routing algorithms. Some of these restrictive rules are listed below.

1. **Antennas** - Are formed by metal traces that accumulate static charge during manufacturing. Without a safe discharge path (through the reverse-biased diode at the output stage of a logic gate) any connected gate may be damaged due to electrostatic discharge. 'Antenna rules' establish maximum allowable ratios of metal area to gate area in the absence of discharge path. The pure router-based solution is bridging (layer-hopping) to limit the amount of metal connected to a gate; this creates more wiring, vias and congestion. The combined router and library-based solution is to drop reverse-biased diodes (source-drain contacts) close to the gate. Tightening of antenna ratios has lowered completion rates of detailed routers and led to more antenna waivers. Should liberal use of dioded cells be required, there will be high costs with respect to chip area and power metrics as well as non-trivial balancing of two sources of yield loss: increased die area versus antenna damage.

2. **Via stacking and minimum area rules** - Arise because stacking of vias through multiple layers can cause minimum area violations with respect to stacking dependent alignment tolerances. Signal routing layers are often divided into local layers, intermediate layers, and global layers. Layers within the same group have same pitches and parasitic. At the highest layer of a given group, the overhang of the 'up-via' can be significantly larger than that of the 'down-via'. In addition, use of multiple-cut via cells to increase BEOL yield is complicated by dependencies on the layers and wire segment widths to be connected.

3. **Width- and length-dependent spacing rules** - Make minimum spacing a function of both wire width and length of parallel adjacencies. This means that edge costs during heuristic search are dependent on path history. Especially pernicious are influence rules (stub rules, halo rules), where a wide wire will influence the spacing rule within its surroundings. This results in strange jogs and spreading when wires enter an influenced area, as well as complicated ECO effects. Another aspect of reliability which is gaining prominence is resist pattern collapse. Resist features collapse upon formation at high aspect ratios. Pattern collapse probability is length-dependent. This contributes to length-dependent spacing rules: longer parallel runs of wires require more spacing. Inserting jogs in the routing can avoid such effects.

Smart Physical Design Tools

EDA physical design tools need to be tied more closely to manufacturing. The implementation of manufacturing issues into design rules and ultimately tech files, which will be read into layout and design tools, is creating new and intelligent generation of physical design tools. By embedding lithography awareness into the design space, adding RET tools to the custom IC and digital IC layout and routing tools and flows, designers are being given interactive checking capabilities that allow them to verify RET compliance during the design phase. Instead of the traditional 'DRV & LVS clean' Tape-out, we are getting lithography and process awareness built in functionality. The main idea is to embed several manufacturing subjects into physical design tools. For example, 'fracturing-aware design' may be a significant feature, whereby OPC, phase-shifter, and functional feature shapes are chosen or perturbed for reduced shot count. Layouts can also be stretched (via insertion of submicron-scale 'dead space') to help definition of major field boundaries (or, soft field boundaries) for mask writing. More complex extraction and characterization capabilities may also be required. Another aspect is physical design flow to consider manufacturing effects. Typically, design mask making and process engineering have depended on rule sets to isolate themselves from having to understand one another's technology. With number and complexity of these design rules exploding and ever decreasing yields, the traditional isolated deterministic design paradigm is breaking down. Close interaction between manufacturing, mask and design communities is inevitable. One of the most important aspects is to ensure predictable printability. New solutions being explored at the design end include regularity. Full chip layouts may need to be assembled as a collection of regular printable patterns for technologies beyond 65nm and 45nm has high likelihood for layouts to look like regular gratings: uniform pitch and width on metal as well as poly layers. Predictable layouts even in presence of focus and dose variations may be required. Several regular layout fabrics have been proposed with varying degrees of performance overhead and flexibility. FPGAs are very flexible but suffer from huge area, power and performance overheads. Via programmable gate arrays offer programmability of logic as well as interconnect using vias and contacts. These offer performance; power and area closer to ASICs as they do not have complex SRAM based programmable logic as FPGAs. Other examples of regular fabrics include Fishbone routing scheme and River PLAs. Somewhat less restrictive regularity can be achieved by more manufacturable cell libraries with regular structures which will require supportive placement techniques.

Before the final tape-out, it is verification time; the very last verification step is mask inspection. Die-to-database method is used to verify that the information on the mask is truly reflecting the design. With mask costs increase, finding defects at mask inspection turns out to be way too late. We now see many tools that inspect designs prior to tape-out, and verify the silicon intent in a simulated image against the original design.

Nevertheless, also this intermediate verification step is becoming too late. The solution is a preemptive check for manufacturing compliance during the physical design phase, cells or blocks, and scanning cell libraries for their adherence to lithography and manufacturing rules. True design-enabled lithography cannot be implemented as a post-design step, but rather needs to be embedded into the layout tools and methodologies, so that designs can be concurrently checked and saved into libraries that are pre-verified for *both* mask manufacturing and silicon printing. New EDA concepts present lithography aware physical design which is fairly new concept function embedded into the mask flow. Hence mask writers work equally hard in perfecting a dummy fill shape, for example a company logo, a gate in a critical path, and a gate in a non-critical path; errors in any of these shapes will trigger rejection of the mask in the inspection tool. The result is overly low mask throughput and high mask costs. Another related objective of physical design can be to maximize the minimum CD tolerance over the whole layout. This can lead to better process window for lithographers as the process window is predominantly determined by the CD tolerance specification. Typically, a process is tuned to print a particular pitch very well. Moreover, this tuned pitch may be changed (for example by changing the nominal exposure) on a design-to-design basis. Physical design tools can then help choose the most critical pitch in the design which needs the most predictable and accurate printability.

Foundries Pre-Check Lithography

In order to handle uncertainties involved in design and manufacturing, new robust optimization techniques were explored. Emerging foundries these optimization techniques were embedded within Lithography process checks as part of custom hardware and software implementations of an additional verification step. After Tape-out layout scan, at the foundry and inside its mask operation, is already too late. Verification of a design for lithography and process compliance needs to happen within the layout editor, while constructing the layout, with an automatic and immediate feedback to the physical designer for compliance. This type of feature requires a model that considers the manufacturing process, and especially the lithography process, to the closest approximation. While foundries use their own OPC and RET models, sharing them with their customer base compromises their IP. Protection of this information is a key element of the strategy for early RET implementation in the design flow. The solution is to encrypt the information, and then selectively allow customers to read certain levels of the information. In this way, foundries can enable their customers to preview their designs, thereby greatly reducing turnaround time, as well as reduce the failure or reject rate at their end.

Lithography-Clean-By-Construction concept has come of age

Even with newer RET methods, the traditional practice of applying these methods to the purely geometric data produced at final tape-out can offer only incremental improvements as design complexity increases. With the help of new EDA tools and flows, designers are starting to embed design information in manufacturing data, permitting downstream tools to optimize analysis on structures that are critical to the design.

At a more fundamental level, however, an emerging class of lithography-aware design tools allows designers to apply more proactive methods to ensure compliance with downstream lithographic requirements. Using sophisticated design rule sets that encode lithographic constraints, these tools allow designers to identify and correct problematic structures well before tape-out (Figure 3).

Using conventional tools, designers typically wait for manufacturing to determine if the design contained any structures that violate RET. Integrated in existing design flows, these litho-aware design tools allow designers to design for RET, OPC and PSM compliance. As designers create edges and place shapes, such tools provide immediate feedback to ensure that the layout will not violate subsequent OPC or phase shifting requirements. That's what we called Litho-Clean-By-Construction process. The system is based on a powerful new methodology that includes lithography analysis inside design flows. Embedded within design process, this powerful new method allows easy, transparent, and highly accurate litho-clean results. This new system, already included within design tools enables designers do not need to become lithography-experts, and neither do engineers on the fab floor have to have ultimate design intent knowledge. Since the technology is embedded within tools, its already automatically checks for manufacturing issues and mainly constraints, that can then be observed by the layout designer, thus creating 'lithography-clean-by-construction' on the fly. In a similar way, litho-aware methods can be implemented within placement and routing tools. The use-model is typically in an interactive way on a cell or block/macro level, with continued checks for RET compliance. In a litho-aware design tools cells will be interactively checked, and batched off into final libraries. In parallel all blocks or chip level run in a batch process to run final signoff verification. With this type of approach, designers can proceed to final tape-out, assured that the resulting manufacturing data is fully lithography compliant. All fab's confidential IP which is embedded within the design flow needs to be protected. This can be easily done using well known encryption methods and limited, tiered access, based on the "need to know" basis information, targeted to the exact user level.

Conclusion

With the advancement of nanometer technologies IC designers are facing significant manufacturability challenges. Traditional methods for ensuring manufacturability like litho-simulations of IC designs are largely ineffective at advanced nanometer processes. In order to deal with sub-wavelength diffraction effects, emerging RET methods impose certain restrictions on the type of structures that can be reliably printed on silicon. In addition new concepts are implemented within design tools to ensure 'litho-correct-by-construction' designs. With the emergence of tools and methods that break down traditional boundaries between design and lithography, engineers can achieve optimal results in the shortest possible time. The continued evolution of design tools and flows that already include lithography-aware capabilities, offers increasingly effective strategies for ensuring manufacturability of more complex nanometer ICs. This new powerful approach used in upstream physical design tools provides a new generation of manufacturability-aware tools for advanced nanometer processes. The foundries are also joining the fight against 'nanometer effects' by providing lithography pre-checks, that are embedded (and encrypted for confidentiality) within design tools, to ensure manufacturability compliance at the design phase. In this way IC design houses are saving the high cost of silicon correction due to process manufacturing issues. No Doubt, it is a constant race after the advancement of nanometer technologies.

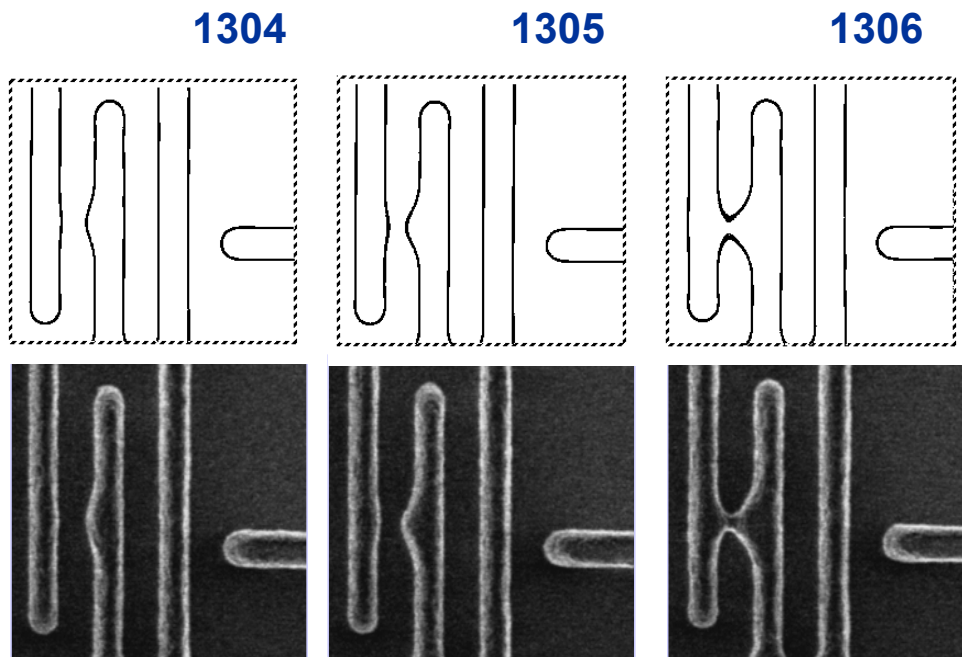


Figure 4: Physical Design EDA tools 'Litho-Clean-By-Construction' approach

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