28nm and below, New Path and Beyond

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Abstract

Increasing complexity and integration, shrinking geometries and consequent physical effects have been some of the ongoing challenges of the nanometer era. Economy condition enforces IC design houses to move to more cost-effective design processes in order to stay in business. Reducing the size of ICs lowers power use, raises performance and reduces the cost, all important benefits at a time when companies want ever smaller devices that do more and cost less. More chip manufacturers begin producing a wide range of ICs with transistors and other components in 28nm and below. What hold companies back from switching to 28nm are the intensive design work and its cost, addressing 28nm process challenges. Design houses can spend months and tens of millions of dollars to verify and tweak their designs in order to comply with the process's complex standards. Introducing advanced design rules, within a wide range of arenas poses acute problems for manufacturing and design verification. The challenges of transitioning to the 28nm technology node are the next chip manufacturing milestones. Experts are in consensus on what will be required to manufacture 28nm and below geometries when traditional scaling techniques are no longer applicable. This paper discusses the challenges of the semiconductor industry, addressing market and design requirements, migrating to 28nm process technology.

Introduction

The intriguing combination of a high performance, low-power process with architectural innovations and cost-effective mass production possibilities, makes 28nm process well suited for power sensitive applications, bandwidth-intensive, and high-end applications. The importance of first-pass silicon is a critical requirement in our today's IC design market. Each advancement in process technology results larger numbers of process layers and transistors, requiring more design and manufacturing rule checks before manufacturing handoff. This results dramatic increase in physical verification runtime and increase in violations analysis, threatening tape-outs deadlines and time to market. The size and complexity of modern designs add another crucial challenge to the current physical design verification technology. Designers need more effective and fast physical verification capabilities in order to deliver accurate results required to keep projects on track. The daunting cost of mask sets for nanometer processes creates additional pressure to detect and correct errors as early as possible in the physical-verification process. Longer physical verification cycles can delay time-to-market, but incomplete rule checking can reduce yield, degrade reliability, and invalidate functionality. The combination of complex rules, more transistors, and extra levels of wiring presents a formidable challenge to today's physical-verification tools, especially when dealing with 28nm and below. Designers can now place multi-million transistors on a single chip and propagate a signal through them at speeds approaching more than one gigahertz. The low-power, 28nm technology platform can provide power, performance and time-to-market advantages for producers of a broad range of power-sensitive mobile and consumer electronics applications.

The Mission: Low Power & High Performance

Current industry standard, conventional process technology has reached its power limit especially within FPGAs and ASICs. Therefore its performance has also reached its limit within low geometries. The cause of the crisis is the *polysilicon* gate and silicon gate dielectric stack that has been used for decades to build transistors in integrated circuits. In order to create faster transistors, semiconductor engineers have continuously decreased the thickness of the gate dielectric layer as the process geometry has become gradually smaller. The reduction of this dielectric thickness has resulted a higher leakage current due to tunneling through the dielectric layer and

leakage current under the gate itself. These effects significantly increase static power with each node improvement in process geometry, creating cost-effected challenge for designers. Process designers are aiming towards efficient management of current tunneling effects developing innovative technologies involved with advanced manufacturing concepts. One of the toughest issues with 28nm node is due to the fact that the gate oxide is very thin. Tunneling effects phenomenon is becoming critical and new materials must be considered for gates especially for gate leakage control.

Foundries are developing new gate dielectric materials with high dielectric constant (k) which allows an increase in gate thickness. The direct result is a new transistor family that can better sustaining tunneling effect.
To solve these problems at 28 nm, Xilinx has adopted a new gate dielectric material

For example, GLOBALFOUNDARIES offers a 28nm technology that is available in super low-power (SLP) and high performance (HP) technology, targeted complex requirements of next-generation SoC's.

The 28nm high performance (HP) and super low power (SLP) technologies are designed for a wide variety of applications from high performance such as graphics and wired networking to low power wireless mobile applications that require long battery lifetime.

Both technologies utilize high k metal gate technology for better control of the gate's channel with high on currents and low leakage current.

The Static Power reduction challenge

"At the 28nm node, static power is a very significant portion of the total power dissipation of a device and in some cases is the dominate factor. To achieve maximal power efficiency, the choice of process technology is paramount because the key to enabling greater useable system performance and capabilities is controlling power consumption," said Victor Peng, senior vice president, Programmable Platforms Development as Xilinx. "We chose the high-k metal gate (HKMG) high-performance, low-power process at TSMC and Samsung Foundry for next-generation FPGAs to significantly minimize static power consumption so we wouldn't lose the performance and functional advantages we get at 28nm."

Power consumption was a global concern and a driven factor within past decades for integrated circuits industry. IC's power consumption is a series factor in the IC design and the operating system. Eliminating access heat, created by ICs and other semiconductors components, directly impacting the entire system's cost due to the usage of cooling fans, heat sinks and other overall temperature regulators. Power has to be carefully designed for device operation and cooling purposes. One of the most critical issues rose due to access heat was the system's reliability. Systems suffered from overheat downtime and high maintenance cost.

The great success of semiconductor industry has been driven by the advancement in transistor technology. The industry could improve the performance of their products by shrinking the transistor dimension, integrating more transistors, significantly reducing manufacturing cost. However, static power consumption has unavoidably offset the cost savings with each manufacturing process reduction. This phenomenon is particularly effects the FPGAs world where modern processes are used in orders to provide high performance at low cost. Systems designed with FPGAs benefit from significant improvements over ASICS, such as rapid-process technology scaling and design innovation, which permit the use of FPGAs in high-availability, high-reliability, and safety-critical systems. Yet, IC's designers can't take complete advantage of deep nanometer processes due to the limitations of static power consumption. In very low processes static power actually exceeds dynamic power in some cases. The solution especially in 28nm node and below is to efficiently manage dynamic power within the entire chip's power budget. Reducing static power consumption allocates more of the power budget for dynamic power, resulting in more functional performance. This method facilitates higher bandwidth interfaces and greater resources for advanced functionality circuits like memories, DSPs and other logic IPs on FPGAs. Efficient management of both dynamic power (Active) and the growing static power (Leakage) is a key factor to a successful design's in 28nm node and below. Wiser utilization of the IC's power budget results higher performance and maintaining the process low cost benefit.

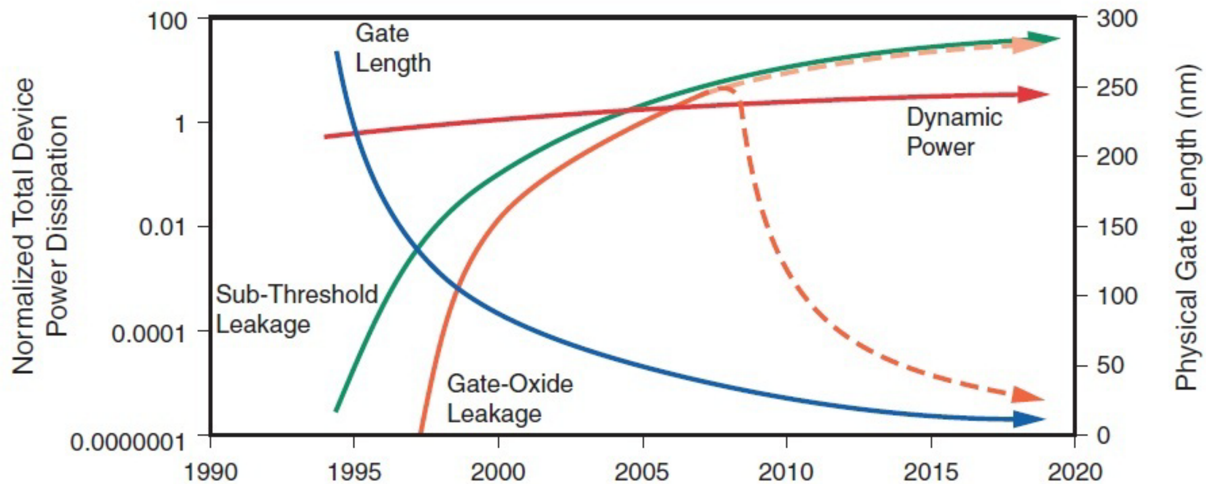

Figure #1 - Dynamic/Static power dissipations inclination

Conclusion: Low Power & High Performance can be achieved

The main objective for advanced process is to reduce power by at least 50% and produce system performance improvements by at least 50% or more. To successfully meet the challenge of increased system performance demands, it is imperative that designers will work closely with customers to identify and understand the architectural obstacle in their systems. External interfacing is one of the typical, major bottlenecks found to be the key barrier to customer's desired performance. To achieve the necessary high interface speeds timing delays and noise margin are critical factors.

The solutions in 28nm and below are investing in advanced clocking technologies and strict datapath design. Tightening datapath structures has a direct impact on the overall system's performance. Efficient parallelism and more pipelining methodologies further improve the system's core

performance. New place & route algorithms and dynamic logic components operation methods are also used for additional power reduction, achieving high performance. Addressing signal integrity with higher precision and resolution ensures reliable functionality and operation although increasing design cost.

Overall, problem can be successfully solved! Given the fact that FPGAs are designed to meet various set of application needs, justifies design's additional cost in 28nm and below. Leading FPGAs companies like Altera, and Xlinix today offering a wide range of 28nm based FPGAs for diverse set of purposes and applications. These FPGAs offers high performance characteristics along with low power consumption in a reasonable cost, making 28nm node a wise choice for a wide variety of projects.

The Reliability Challenge

With manufacturing processes advancemans it becomes imperative for the semiconductor industry to critically address the issues that the new age has brought with itself. High speed and low power are not the only targets that designers have to design for. Specifications now include additional functionality and consistent performance. With 28nm node and below the performance variation caused by a process variation is much larger. The development of semiconductor technology in the next decade will bring a broad set of reliability challenges at a pace that has not been seen in the last 20 years.

Many aspects of semiconductor design and manufacturing will undergo dramatic changes that threaten the nearly unlimited lifetime and high level of reliability that customers have come to expect even as product complexity and performance have increased. The introduction of new materials, processes, and novel devices along with voltage scaling limitations, increasing power, die size, and package complexity will impose many new reliability challenges. Current reliability issues are worsens causing designers to struggle with new level of critical risks. With structures on the chips becoming smaller and the number of such structures increasing exponentially, even if reliability and manufacturability of the structures remains same, total reliability of the chip goes down. More number of structures increases the probability of failure on a chip, particularly in 28nm node and below.

"Within high-k gate dielectrics, metal gate, copper/low-k interconnects, the

introduction of new materials, processes, and devices presents challenges. Bulk material and interface properties usually define the intrinsic reliability characteristics while defects establish the extrinsic reliability characteristics. Process integration flow, techniques, and process tools often create first order reliability effects (both intrinsic and extrinsic). The importance of characterizing these materials and processes for reliability as well as for performance during the early development stage cannot be overstated. System-on-chip (SOC) products that typically integrate new function and often include large memories (SRAM, DRAM, and Flash) bring about unique design, integration, and test challenges. Microsystems require consideration of a wider range of failure modes than microelectronics alone and introduce new failure modes because of the interaction of diverse technologies that would not be present if each technology were manufactured on a separate chip.

In addition, optical, chemical, and biometric sensors and micro machines (MEMs) require the development of new accelerated tests and failure mechanism models.

Electrostatic discharge (ESD), latchup, and packaging in the nanometer regime also raise reliability concerns. Even though ESD and latchup effects have been well characterized for many years, scaling brings about new issues and concerns. Similarly, the increased complexity and performance requirements for packaging these products act as an exponential multiplier for many of the failure mechanisms besides introducing new ones. Finally, two critical crosscut issues are related to design and test. These may be the more difficult challenges as the work needed to reach solutions is typically dispersed across many organizations, sites, and partners. Integration efforts tend to be less focused than material and device issues. Although the challenges may be clear, the paths to find solutions tend to be fragmented and obscure; consequently, these items require special research focus. This document is neither a complete nor exhaustive list of reliability challenges for the ITRS.

Certainly any area of technology advancement includes its own set of potential reliability problems and new challenges. Instead, those broadest or most critical challenges are highlighted." **The International Technology Roadmap for Semiconductors (ITRS) - Critical Reliability Challenges for the International Technology Roadmap for Semiconductors (ITRS); March 2004**

Reliability is becoming a critical concern in 28nm process for manufacturers and designers of integrated circuits. Developing practical, affordable techniques to ensure reliability constraints has always been an ongoing

challenge. With these new advanced processes it is even more challenging, as problems require the introduction of new materials, new operating regions and the reduction of reliability margins.

Successful modern nanometer design requires reliability analysis built-in flow. Manual and routed interconnections must be reliability aware, taking physical effects such as SI into consideration on-the-fly. They must also be manufacturing-aware, with capabilities such as variable-spacing and variable-width routes to support copper, CMP, and sub-wavelength processes. Silicon integrity and reliability have become first-priority effects for successful tapeout. For the past decade the EDA industry has provided extensive solutions for reliability phenomenon, yet significant improvement is needed in order to efficiently provide a unified solution in 28nm node and below. Since reliability and signal integrity issues are directly connected, it creates great difficulties to achieve a comprehensive solution within EDA tool.

In order to overcome advanced processes reliability challenges new approaches have arise. Instead of performing a global RV analysis, on a large layout blocks, an early stage, interactive checks are made. Designers can detect and correct reliability issues early in the design phase approaching signoff ready condition. Especially during custom and semi-custom layout design stages an early detection of reliability issues lead to a higher quality correction, achieving DFM-Aware physical design and higher yield.

Physical Verification – Major Bottleneck

At 28nm and below designers can no longer rely on the typical physical verification methods to deal effectively with the complex rule decks and massive data sets associated with deep nanometer designs. EDA companies are constantly presenting with newer concepts to physical verification attacking new set of constraints and requirements, delivering capabilities that reduce violations correction time for today's increasing designs. These new verification methods are aimed for 'look ahead' concept, trying to save significant design time, causing resources saving, while also provide rules simplifications. Although EDA technologies are rapidly 'chasing' nanometer technology it does not provide an entire set of solutions. Corporations are enforced to develop in-house methods, concepts and even software in order to find compromising solutions to their deep nanometer issues. Accuracy is

insufficient. Today's physical verification methods force engineers to work via long design verification process before detecting design violations information. This delays development cycle, forces additional iteration cycles, and worse of all tape-out schedules! As design is scheduled to tape-out at a certain date but has to pass final verifications (For example: Reliability Verification), the chance of last minute corrections is very high and may results tape-out delay of days up to weeks or even months. (Depend of type of potential violations that have to be fixed.) The new trend of verification solutions delivers design violations information embedded into the design stage and debug environment concurrently with the physical construction process. In a way it is some sort of predicted information to accelerate violation correction time and reduces the number of repeated verification cycles. Beside more efficient design analysis the new methods are focused on performance increase which significantly reduces the duration of verification iterations, speeding the development of nanometer designs. EDA vendors are constantly working in these two major arenas, effectiveness and speed!

Since traditional physical verification approaches and methods like conventional hierarchical, multi-processing model have become not sufficient for deep nanometer technologies, a new direction for physical verification come of age. The industry demands new solutions that are made of integrated methods. A new scalable approach can successfully handle large design size, nanometer challenges and rule deck complexity with greater efficiency, incorporating multiprocessing and better database management. Newest physical verification concepts present new partitioning methods that remove multiprocessing limitations inherent to today's EDA tools. The development of advanced partitioning concepts has lead to high level of utilization across massively parallel computing resources. The new approach is based on compilers optimization to implement a combination of partitioning strategies that achieve an efficient usage of parallel processing resources. This approach enables the analysis of the design and rule deck during compile time to define and allocate processing tasks across available computing resources according to a variety of factors like priority, partition nature, etc'. This efficient task allocation approach optimizes the processing implementation to achieve performance and accuracy. This advanced partitioning technique is based on exclusive combination of rule deck terms, design characteristics and available computing resources to achieve an efficient resource leveling across large compute farms, eliminating long poles and speeding runtimes. Using this approach significantly increases overall system performance potentially utilizing unlimited amount of CPUs.

Another new direction within recent verification approaches is to provide private high-level commands to handle specific complex checks. For example signal integrity issues such as reliability and density checks. These private high-level commands are replacing long sections of primitive commands that complicate rule decks authoring and causing processing delays. One can say that now we have a system that is construct of dedicated processing engines that analyzing each partition according to its characteristics. (Size, type of circuitry, Etc') There is no need to rewrite rule decks. The optimizing compiler automatically detects opportunities to allocate dedicated engines based on recognition of pre determined patterns in the input rule deck. In this way the tedious work of rewriting rule decks is avoided. Another major advantage of this approach is accuracy improvement. Due to the fact that each engine is designed for a specific verification task, (according to partition characteristics), the end results is much higher accuracy level. One can say that each dedicated engine is an 'expert' in his field. It is designed to process a certain type of data rather than relying on the approximations inherent in a sequence of primitive verification operations. For example, in a reliability check mentioned above, tools using conventional primitive-level commands will not be able to detect situations that a specific engine would do. Combining private commands for dedicated processing engines is a strong solution for advance nanometer challenges. In this way newest, complex nanometer effects can be efficiently handle, fast! These private commands implemented as dedicated processing engines take few lines, replacing potentially hundreds of lines in a typical rule deck, dramatically improving rule deck development and maintenance.

Another example in the DRC verification domain is using flexible mathematical expressions to replace the single-dimensional measurements of traditional DRC. An equation-based design rule definition technique provides multi-dimensional feature extents that can reduce the number of rules, improve rule's accuracy and reduce complexity and run time. In addition equation-based DRC analysis significantly improves DRC debugging capabilities, offering higher quality physical layout construction and improving yield. One of the most significant characteristics of this method is the capability to implement advanced technology checks besides geometrical rules like connectivity, DFM and more. The customizable physical modeling capabilities using equation based DRC enable foundries and chip designers too quickly and efficiently adapt 28nm nodes and below. With the new modern geometries there is a major leap in design rule capabilities which creates challenge to the industry regarding how DRC rules are defined, documented, implemented and debugged.

Data management is essential especially at 28nm and below! As the industry is moving forward with modern nanometer technologies new phenomenon are imposing more constraints on upstream design characteristics. One of the major issues is the data management. Industry's EDA verification tools are adopting an open architecture approaches such as OpenAccess for data management. The optimization of design data model is a key factor for overall system performance. Another essential factor is the ability to reduce the 'time per violation' factor which provides an important advantage in decreasing the number and magnitude of design iterations common in today's physical verification environments. OpenAccess-based physical verification tools write violations to the design database as they are discovered, permitting early identification of design errors. Therefore, if designers find serious violations as a verification run progresses, they can terminate the run and immediately begin working to fix these violations. This means major time savings during physical verification, achieving clean design with much less iterations.

Physical Design interactive solutions

Even with newer physical verification methods, the traditional practice of applying these methods to the geometrical data produced at final tape-out can offer only incremental improvements as design complexity increases. With the help of new EDA tools and flows, designers are starting to embed design information in manufacturing data, permitting downstream tools to optimize analysis on structures that are critical to the design.
At a more fundamental level, however, an emerging class of Rules-Aware design tools allows designers to apply more proactive methods, during IC layout data construction, to ensure compliance with modern nanometer processes requirements. Using sophisticated design rule sets that support wide range of constraints, these tools allow designers to identify and correct problematic structures well before sign off stage.
Using conventional tools, designers typically wait for sign off verification to determine if the design contains design violations. Integrated in existing design flows, these Rule-Aware design tools allow designers to design for DRC, RV and DFM compliance. As designers build their layout and place/edit shapes, such tools provide immediate feedback to ensure that the layout will not violate subsequent DRC, RV or DFM requirements. That's what we called Rule-Aware, Clean-By-Construction process. The system is based on a powerful new methodology that includes design rules, of few fields, analysis inside design flows. Embedded within design process, this powerful new

method allows easy, transparent, and highly accurate design-rule clean results. These new systems, already included within design tools, enable designers do not need to become rules-experts and to have ultimate design intent knowledge. Since the technology is embedded within tools, it's already automatically checks for process requirements and constraints that can then be observed by the layout designer, thus creating 'Rule-Aware' layout on the fly. In a similar way, DFM and litho-aware methods can be implemented within custom and placement and routing tools. The use-model is typically in an interactive way on a cell or block/macro level, with continued checks for design rules compliance. In a Rule-Aware design tools cells will be interactively checked, and batched off into final libraries. In parallel all blocks or chip level run in a batch process to run final signoff verification. With this type of approach, designers can proceed to final tape-out, assured that the resulting design rules and manufacturing data is fully compliant. All fab's confidential IP which is embedded within the design flow needs to be protected. This can be easily done using well known encryption methods and limited, tiered access, based on the "need to know" basis information, targeted to the exact user level. Today EDA vendors are offering robust technology to provide Rule-Aware design environment in major bottleneck verification arenas. For example, Micrologic Design Automation (www.micrologic-da.com) nanoToolBox™ offers today a wide set of interactive tools enabling interactive verification of DRC and RV during construction stages of IC layout. The results are provided on-the-fly and allow designers to correct them in early stages of layout design, improving the layout quality and significantly reducing sign off time!

Conclusions

The IC design world is in a constant race after nanometer technologies progress. With each new process designers face a whole new world of constraints and effects. This fact enforces EDA vendors to constantly develop new solutions and approaches for industry's needs. As the process moves into 28nm and below the current physical verification tools do not provide sufficient performance and accuracy. Consequently designs do not meet their tape-out schedules and furthermore, fail in basic functionality. New methods were developed to address deep nanometer design requirements. These methods are a combination of enhanced performance and open data architectures allows design teams to broaden the scope of physical verification checks to address complicate nanometer manufacturing issues that have a significant impact on yield. In addition, major efforts are put into

early stages, interactive technologies to identify design violations during the construction of IC layout database. Designers no longer need to wait days for the minimum set of results that enables design signoff. Instead of waiting days for verification results that enable design signoff, an interactive analysis in DRC, RV and DFM fields identifies issues during layout construction, enabling designers to perform an efficient correction and make a direct impact on the quality and yield. These new approaches in physical verification greatly enhances the designer's ability to deliver successful high yielding designs that work on the first mask set, which is a significant payoff in the era of few thousands design rules, one billion transistors, and few million dollars mask sets.

No Doubt, the industry’s emerging nanometer technologies virtually cannot be fully utilized and exploit without new approaches in physical verification.

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