Challenges & Solutions of Signal Integrity in VDSM Physical Design

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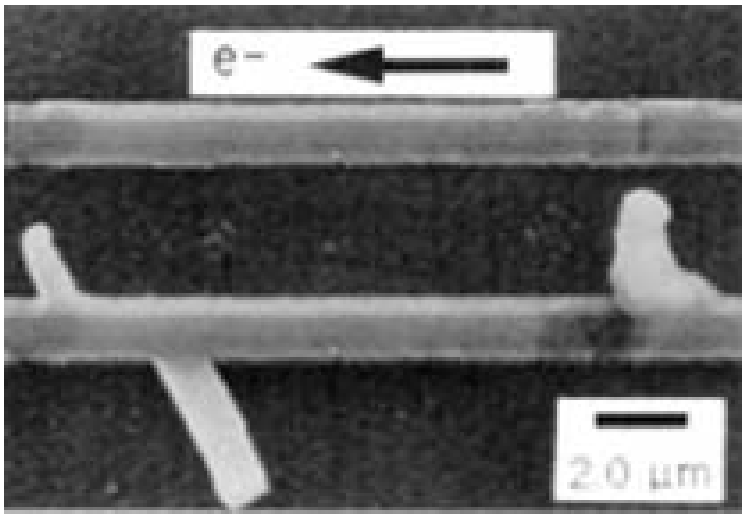
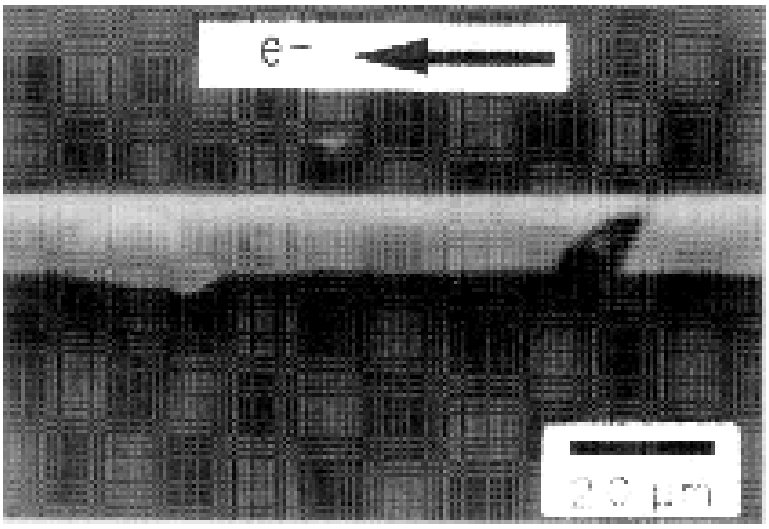
Abstract - Today's nanometer design geometries put tremendous pressure on IC's design houses to maintain advanced design flows to achieve satisfactory level of predictability and productivity in the chip design process. Existing EDA design tools and methodologies are in constant race to address these issues effectively. Although timing closure remains the major challenge, it is greatly affected by very deep sub-micron (VDSM) processes phenomenon like signal integrity, power consumption, and testability. The incorporation of signal integrity solutions into the IC design flow has become a necessity. The 'Signal Integrity' term refers to a broad set of integrated-circuit design issues, such as electromigration, crosstalk noise, IR drop, and manufacturing-related problems. (for example antenna effects) As the technology is moving forward variations on a single die complicate the design process. In order to achieve a successful tapeout, in reasonable schedules, reliability and signal integrity must be resolved during the design flow.

Electromigration - Very Deep Sub Micron designs contain millions of devices and operate at very high frequencies. The current densities (current per cross-sectional area) in the signal lines and power are consequently high and can result in either signal or power electromigration problems. The electron movement induced by the current in the metal power lines causes metal ions to migrate. That phenomenon of transport of mass in the path of a DC flow, as in the metal power lines in the design, is termed power electromigration. There are two types of electromigration. Uni-Directional, for example power and static signals and Bi-Directional, for example clocks and other switching signals. The most critical is the Uni-Directional electromigration type since the electron 'erosion' move constantly in one direction and can cause signal line failure. The power electromigration effect is harmful from the point of view of design reliability, since the transport of mass can cause open circuits, or shorts, to neighboring wires.

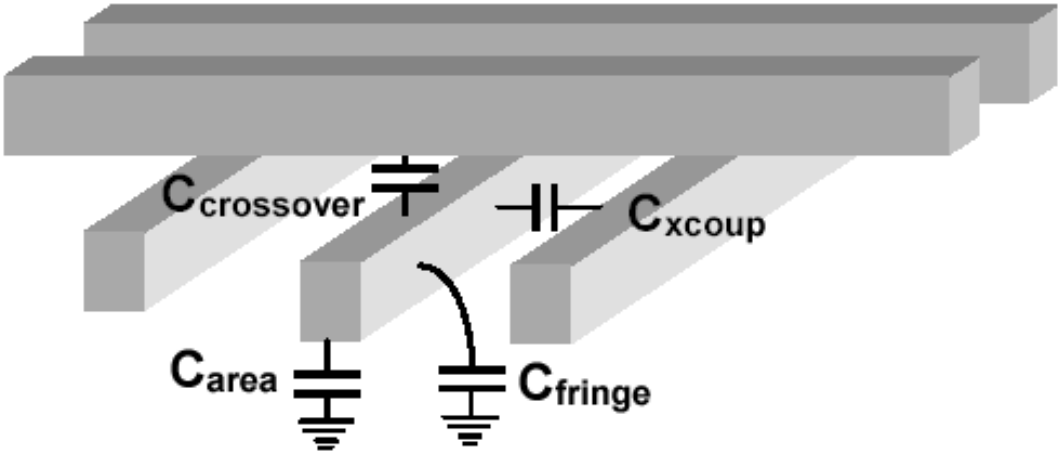


Electromigration Effect – Short Circuit
Image: Computer Simulation Laboratory

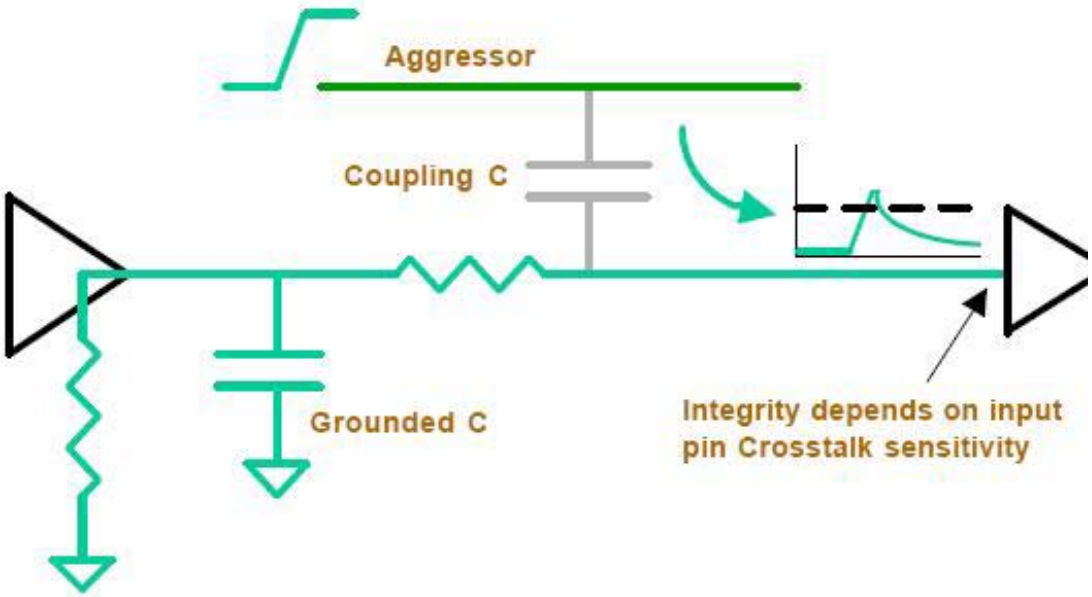


Electromigration Effect – Open Circuit
Image: Computer Simulation Laboratory

Crosstalk - With the scaling of the horizontal dimensions of wires, the aspect ratio of the horizontal to vertical dimensions is reduced, resulting in increased ratios of coupling capacitance to ground capacitance (over or under crossovers or to substrate). A significant crosstalk noise may occur due to the relative rate of switching (rise and fall times of the signals) and the amount of mutual capacitance. Crosstalk noise, depending on its amplitude and its timing may cause false switching or delays. The ability of a physical design environment concurrently to analyze and correct for these various signal integrity problems during a physical implementation flow is highly dependent on the design system architecture. An integrated design system is necessary to address VDSM phenomenon efficiently and to provide design closure in a timely manner.



Crosstalk Noise
Image: Magma Design Automation



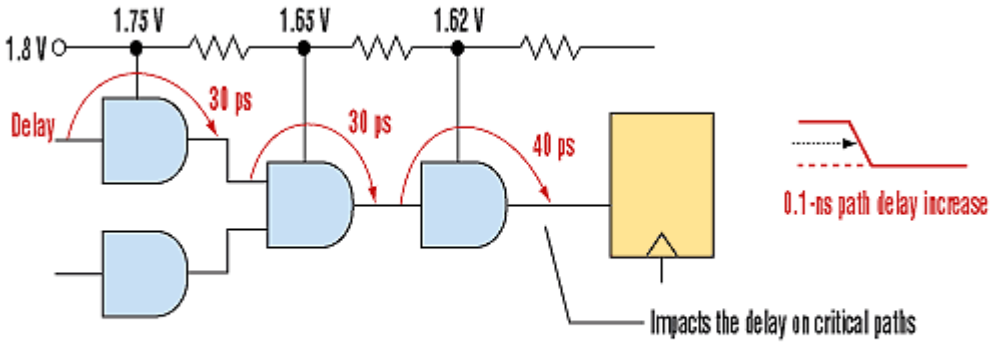
Source: Cadence Design Automation

This diagram above shows a crosstalk induced logic error. In this case, the 'victim' net is trying to maintain a logic value zero. The aggressor net switches from a low to a high value, which couples a glitch into the victim line. If the glitch is big enough, it can exceed the logic threshold of the receiver on the victim line, and be recorded as a one rather than a 0. A faster aggressor transition or a bigger coupling C will cause a larger glitch. A stronger driver (lower drive impedance) or more grounded capacitance will reduce the size of the glitch. For long lines, the wire R also comes into play, with the higher wire R from the longer wire leading to a larger glitch. Note that the true parasitics are distributed over the length of the line. They are shown as lumped values in the diagram just for sake of simplicity. Either lumped or distributed models can be used in analysis – the lumped models by necessity are conservative, and report more errors, but the distributed models require much larger data volumes.

Timing – As technology moves into VDSM arena, new timing challenges occurs. One of the serious issues is inadequate modeling of nonlinear waveforms and variations in input pin thresholds which cause inaccurate interconnect delays and curious modeling anomalies like negative cell delays. Timing is dominated by interconnect dependent RC delay especially in VDSM designs. Effects like cross coupling, inductance, via resistance, power integrity and wire self-heating become first-order design parameters. Design flows using various point tools fail to predict final timing during early stages of the design which leads to unnecessary cycles of re-simulations. The ever-increasing complexity of system-on-chip design, coupled with uncorrelated tool flows, makes it more difficult to achieve design closure on all fronts. Advanced tool capabilities are needed to ensure that

all aspects of the design, from timing closure to signal integrity to power requirements, are addressed simultaneously to ensure on time silicon delivery.

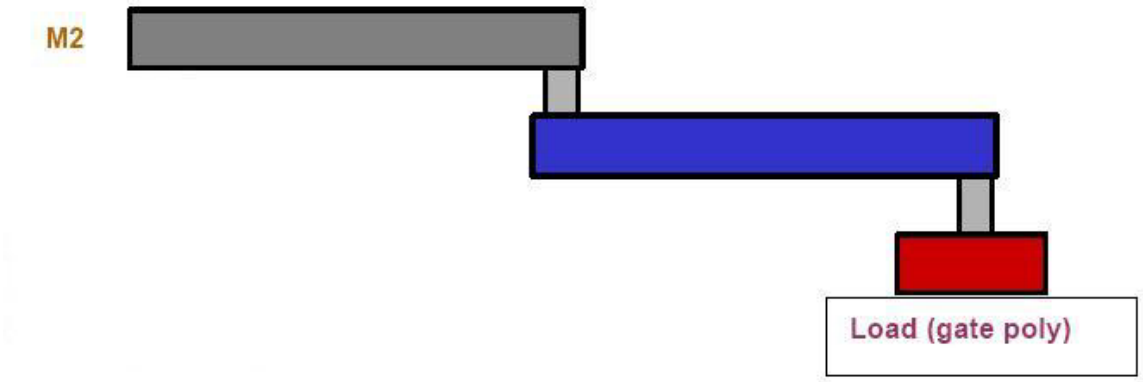
IR Drop - One of the major issues of signal integrity is the IR drop effect. IR drop is a signal integrity effect caused by wire resistance and current drawn from the power and ground grids. If the wire resistance is too large or the cell current is higher than predicted, an undesirable voltage drop may happen. The voltage drop causes the voltage supplied to the affected cells to be lower than required, which leads to larger gate and signal delays (TPD), which in turn can cause timing discrepancies in the signal paths as well as clock skew. Voltage drop on power and ground grids can also affect the noise margins and compromises the signal integrity of the design. Therefore special attention should be taken to resolve the IR drop effects during post-layout phase.



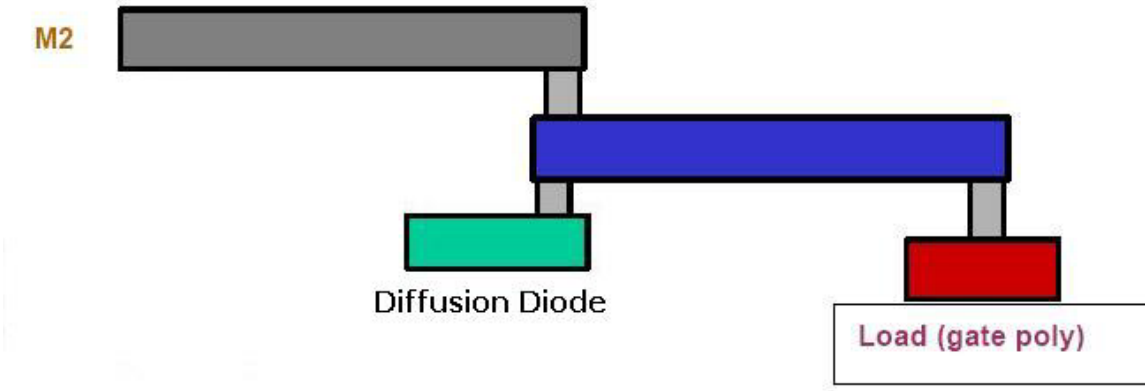
Voltage drops through a chain of logic gates can severely influence SoC timing closure. Here, 0.1 ns of additional delay, which may not have been accounted for in static timing analysis, is imposed by an aggregate drop of less than 200 mV.

Image: Magma Design Automation

Manufacturing Effects- As the nanometer technology evolves, manufacturing related problems become a significant factor in IC's design. Antenna and metal fill are two of the manufacturing concerns that must be addressed during the physical design phase. The antenna effect occurs during the manufacturing of IC's. During the metallization steps, wires connected to the polysilicon gates of transistors in the design, collect charge due to the ion-etching process. The voltages on these wires can exceed the polysilicon gate breakdown voltages damaging the gate. Manufacturing design rules limit the amount of interconnect that can be directly attached to a gate, as the total area and perimeter of interconnects are factors in how much charge builds up. In additional it's common practice to connect small diodes to sections of interconnect to provide a discharge path for charge generated during the manufacturing process. With the use of such diodes, larger sections of interconnect can be attached to a MOS transistor's gate eliminating the risk of antenna effect.



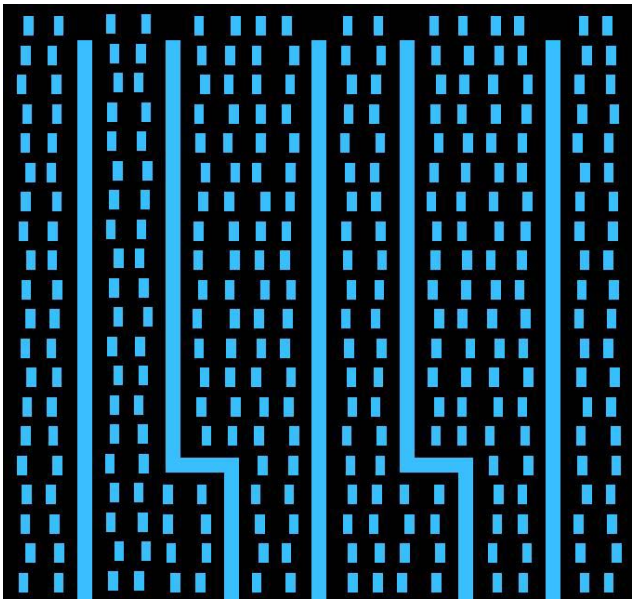
Antenna Sample – The routing path from Polysilicon through Metal1 and Metal2 can cause Metals charge collection due to the ion-etching process.



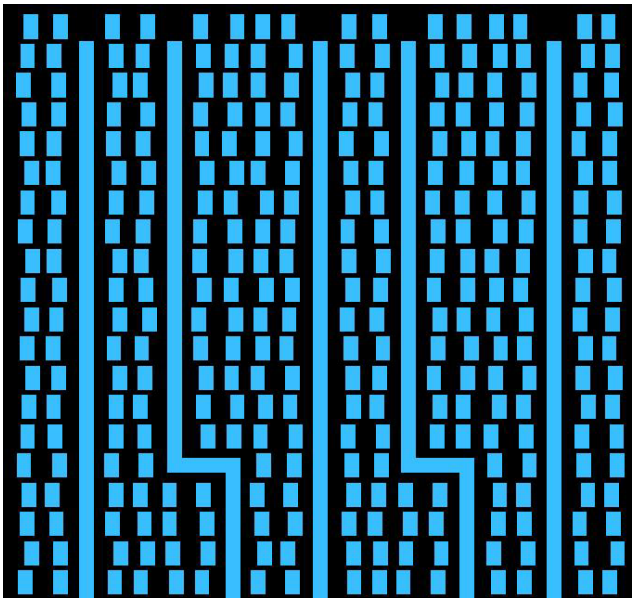
The Solution – Connecting Discharging Diffusion Diode

Another significant manufacturing issue is metal density. The difference in oxide heights for a given region on a design called Planarity and is an important factor affecting the wafer yield. When a design has regions of low metal density, the oxide layer can sag considerably. Polishing does help improve planarity, but if metal density is particularly low, the amount of oxide sagging can be too great to overcome. Metal fill is required to maintain a uniform metal density across the chip on each layer and thereby ensure planarity during the chemical-mechanical polishing process. There are few accepted

methods of creating metal fills. The simple yet tedious way is to insert it manually through a layout editor; this is time-consuming and error prone process. A second approach is to use automatic insertion methods in layout or place-and-route tools. (This is the most common way today) Although this approach is certainly faster and easier, grid restrictions and other issues often limit the amount of metal fill that can be placed. The third approach is to do automatic metal fill insertion at the time of physical verification. This is considered to be the most efficient way since the density checking and metal fill repair can be done in a single iteration.



Low Density Metal Fill
Image: University of Delaware (Engineering)



High Density Metal Fill
Image: University of Delaware (Engineering)

In many today's IC design approaches signal integrity analysis is performed as a post-layout activity. Analyzing and correcting these issues prior to the physical design phase often results in costly and time-consuming design iterations, slipped schedules, reduced product performance and in some cases larger die sizes and poor yield. It is recommended to have a single data model and an integrated, unified design system to improve productivity and ensure predictable design schedule. In the nanometer era, signal integrity must be addressed as an integral part of the design flow. The demand from EDA tools manufacturers is to provide a solution in early stages of the design. The electromigration and crosstalk correction should be done during the placement phase. The design must be well-tuned, with comparable slews, drivers matched to loads and no long resistive wires. During post-processing phase extraction and wires modeling must be aware of metal filling that will be applied. Using this approach, IR drop analysis in post-layout phase may give accurate results to ensure appropriate signal integrity. Using a single, unified data model, the design flow should be based on the same data model from start to end to address nanometer-design challenges.

If we are examining some signal integrity 'real-life' samples we can clearly see that the majority of these issues can be fixed early in the design flow. For example, electromigration violations can be corrected early in the design flow once global routes are available. Continuing with the remainder of the design flow, wire widths, layer assignments and cell routing consideration can be maintained, and new violations that may be discovered can be fixed incrementally. This process fixes predicted electromigration violation ahead of time and constantly continuing to correct new violations as we go throughout the flow. In similar way, performing IR drop analysis within early placement results can drive optimization in the remainder of the design flow regarding voltage related cell delays. One example is the typical input-to-output logic gate delays that are affected by power and ground voltage-drop effects, which are not accounted for in traditional timing analysis. These types of delay may result critical paths failure and significant amount of iterations within the design flow. Preventing and correcting crosstalk delay should be done as early as possible in the design flow. This can be done by shortening critical paths and balancing skew across the design during physical synthesis. After clock networks synthesis is done, hold fixing and setup optimization with crosstalk delay can be performed. The optimization process should cover crosstalk effects, IC's variation, power, voltage drop and other signal integrity effects. In the recent few years EDA vendors successfully provide such capabilities within design platforms. (Mentor Graphics; Calibre, Cadence; Silicon Ensemble)

As IC's manufacturing process rapidly shrinks crosstalk noise becomes one of the primary concerns for designers because it significantly impacts the signal integrity. Today's EDA technologies help to ensure that the resulting physical design achieves signal integrity and timing closure simultaneously. This is achieved through concurrent crosstalk analysis and layout optimization in conjunction with timing optimization. Potential crosstalk problems are being addressed early on during the physical design

process, not after the process, with a set of precise pruning strategies, accurate LPE, and a comprehensive set of crosstalk prevention/repair measures. The newest EDA technology allows users to specify various crosstalk constraints such as maximum total coupling capacitance, timed peak noise voltage, peak noise voltage, and maximum parallel length for a wire. These constraints work in connection with the pruning strategies in the crosstalk analysis to accurately pinpoint wires with potential crosstalk problems and to drive place and route to prevent and/or repair them with appropriate measures.

Signal Integrity issues should be analyzes and correct throughout the design process. The capability of a design system to take into consideration these issues is highly dependent on its architecture. It is the conclusion of this paper that the analysis and correction of signal integrity issues must be embedded within an integrated design system based on single data model. This will significantly improve the design flow productivity, leading to on time delivery and satisfactory time to market factor.

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