Deep Nanometer Range
The Transitioning to the 45nm technology and below

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June 2006

The challenges of transitioning to the 45nm technology node are the next chip manufacturing milestones. Experts are in consensus on what will be required to manufacture 45nm and below geometries when traditional scaling techniques are no longer applicable.

There is no doubt. The move to the 45nm process node will be costly and challenging, but worth it for future applications. Despite steep design and fabrication costs, experts are generally optimistic about the ability of EDA and foundry providers to come up with solutions, and of designers to leverage their investments in 45nm technology through intellectual property reuse.

While these industry leaders all agreed that 45nm is not a matter of scaling alone, they each have a unique perspective on how to address the challenges of reducing power consumption, lowering leakage current and solving the gate materials issues. As advances in semiconductor process technologies become more complex, time consuming and expensive, companies around the globe are creating 'subject related' partnerships in order to share cost burdens and accelerate development, while raising system performance and quality.

The estimations are that by 2010 45nm technology will be mature enough, and have enough design tool support, to attract a broader range of applications. A direct derivative of 45nm design and manufacturing high costs will be the complexity of verification and DFM EDA tools. EDA tools and flows will have to evolve into a new era which of course will increase the cost for chip designers. Designers will have to leverage their investments through reusable architectures and IP, thus amortizing the cost across multiple products. The prediction is that an entire set of design tools will have to be developed especially for deep Nanometer range. (45/32nm)

The costs of 45nm will raise the stakes. In order to be successful, designers will have to be relatively certain of first pass success. This can be achieved through the diligent efforts of everyone in the tool chain. The business organization of EDA vendors hampers the development of solutions. The challenges of 45nm design include density, leakage, and most of all, return on investment. Another challenge is the aging mindsets like design rule manuals, or SP&R (synthesis, placement and routing) handoff to manufacturing. Those are really showing stress at 65nm and probably won't survive the transition to 45nm. In addition manufacturing variability may cause excessive guard-banding and uncertainty.

When it comes to 45nm process, the Physics aspect is becoming a crucial factor. The typical scaling is translated into more exact specifications for 45nm and below. As feature dimensions decrease, so, too, must process tolerances and measurement precision. For example, 20nm features are smaller than the dimensions of the interaction volume of the electrons at typical beam energies, and the intensity profile of such a feature is no longer a sufficiently accurate representation of its physical shape. Accurate and repeatable measurements require reduced energy and detailed physics-based modeling of beam-sample interactions. The growing demand for

measurement capacity comes through process control improvements. Gate length determines device speed, and variability in speed leads to cumulative errors in circuit timing, which further degrades overall operational speed. Improvements in process control lead directly to higher speed and higher aggregate product value through higher prices for premium performance.

The physics of 45nm is causing the process complexity to increase by the introduction of new materials that dictate new metrology requirements. For example, the photoresists used with ArF lithography light sources shrink significantly when illuminated by electrons with energies >100eV. Accurate measurements require unconventional electron optics that maintains resolution at ultra-low voltage. As process technology becomes more complex, so must the techniques used to control it. The next few years are likely to see a proliferation of technologies specialized for particular tasks. For CD process control, this will likely mean the combined use of CD-SEM, optical CD, CD-AFM, and FIB/SEM technologies, which will ultimately be seen as complementary, rather than competitive.

The industry is anticipated to reach 45nm node and below by the end of the decade. This will occur in a large part, due to a continuing acceleration of the flow of innovation, mostly from the bottom up. While the industry faces unprecedented technical challenges, it has also seen significant consolidation and domination by a relatively few large companies. These large companies compete well in a market where cost reduction through economy of scale is a primary consideration. With more complex devices, structures can no longer be regarded as simple 2D layers. Control of 3D shape has become critical as well. Moreover, features cannot be considered in isolation. Proximity effects due to the presence or absence of nearby features play a significant role in processes ranging from lithography to CMP. Controlling these effects requires in-circuit measurements.

An increasing need for metrology capacity is also expected. With the introduction of more complex processes, more ways to fail are created. In order to control this phenomenon, manufacturers are adopting larger sampling plans and face expensive measurement technologies, increasing demand for measurement capacity in a competitive environment that will not tolerate price increases to recover the added expense. This increases the pressure on equipment manufacturers to improve efficiency and lower total cost-of-ownership.

There is no debate that 45nm and 32nm technology will occur; it's a matter of what the technology will look like.