Design for Manufacturing (DFM)

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February, 2005

Abstract

Design for manufacturing has become one of the key factors of VDSM designs for the past decade. The necessity of corrections optical process effects (optical proximity correction (OPC) and phase-shifting masks (PSM)) creates entire layout design and verification methodologies. Classic DFM design (Design for Manufacturing) consists of an analysis of yield and a set of constraints. These constraints are imposed as both guidelines and by creating an MRC (manufacturing rule check) deck.

Reticle enhancement technologies (RET) like optical proximity correction (OPC) and phase shift masking (PSM) have significantly increased the cost and complexity of sub-micron nanometer photomasks. The photomask layout is no longer an exact replica of the design layout. As a result, reliably verifying RET synthesis accuracy, structural integrity, and conformance to mask fabrication rules are crucial for the manufacture of nanometer regime VLSI designs. New EDA systems consists of efficient wafer-patterning simulators that is able to solve the process physical equations for optical imaging, resist development and hence can achieve high degree accuracy required by mask verification tasks. These tools are able to efficiently evaluate mask performance by simulating edge displacement errors between wafer image and the intended layout. Our discussion addresses the necessary changes in the design-to-manufacturing flow, including infrastructure development in the mask and process communities as well as opportunities for research and development in IC physical layout and verification stage.

Introduction

In the nanometer era, which the wavelength of lithographic printing is greater than the design half pitch (sub-wavelength design), a new paradigm is required for a manufacturing-aware design – one that affects the design flow fundamentally and also adds much complexity to the mask data preparation (MDP) process. As designs step into 90 nm, 65 nm and below they can be characterized by a significant reduction of lithographic contrast, K1 (Figure 1). This creates a whole new world of implications. One of the major issues is that the lithographic process is not synchronized with the original physical design pattern. Even at perfect imaging focus and exposure, results in fabricated IC pattern elements that are no longer a faithful replica of the original physical design. In addition, manufacturing margin is much reduced. This phenomenon has a direct impact on the cost due to the fact that new methods have to be invented to recover some of the imaging fidelity, improving the range of focus and exposure that produce accurate thin film patterns on silicon.

The sub-wavelength gap

These goals are partially achieved by modifying MDP to include resolution enhancement technologies (RET). These technologies modify the mask shapes from those of the physical design such that the fabricated shapes are much closer to the physical design, while the shapes on the mask themselves are an input to the highly nonlinear transformation caused by the low K1 lithographic systems. Successful RET strategies also solve the second issue, that of manufacturing tolerance. When this strategy is well implemented, the result is more exact fabrication that is more correlated with the design intent, and with much improved yield in the presence of variations in manufacturing parameters.

In the high K1 area, mask shapes are equal to actual silicon shapes and also print with good manufacturing tolerance. Figure 2 shows the classic design and mask data preparation flow, in which the physical design data, usually represented as a GDSII stream file, is representative not only of the designer's intent, but also the mask shapes. Figure 1A shows the sub-wavelength gap.

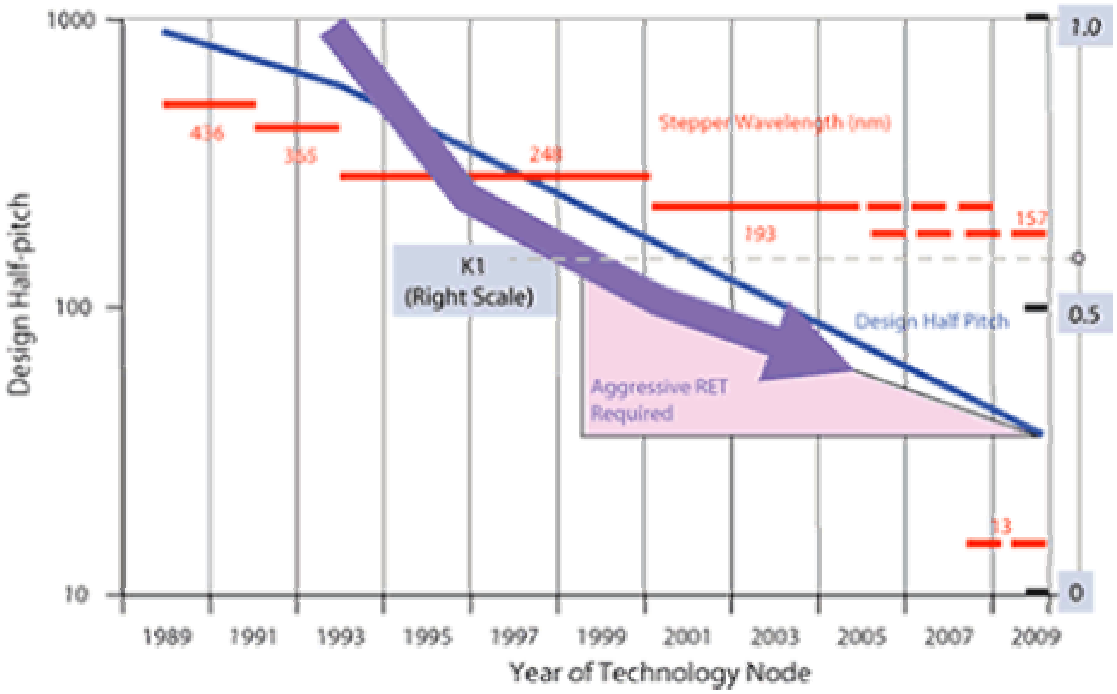


Figure 1 - New era of sub-wavelength design
Source: Montgomery Research

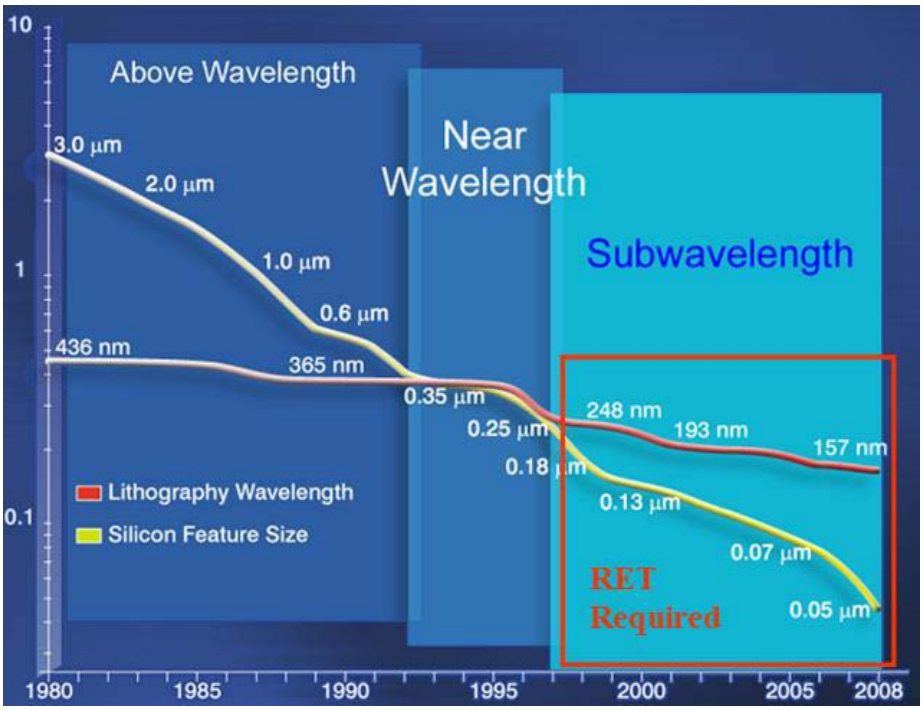


Figure 1A – The sub-wavelength gap
Source: Numerical Technologies

RET implementation

Reticle enhancement technologies for VDSM (Very Deep Sub Micron) integrated circuit manufacturing has dramatically complicated the mask data and increased the cost of advanced photomasks. The increase in pattern complexity due to optical proximity correction (OPC), the tight requirements for Critical Dimension (CD) control, and the difficulties in defect inspection and repair all contribute to the manufacturing cost increase. For phase shift masks (PSM), the problems are compounded by additional requirements such as controlling the etching of multiple materials, alignment of multiple layers, and inspecting small defect with weak signals. In addition to the added complexities in mask making, the growing array of Reticle Enhancement Technologies (RET) also put more constraints on the physical layout design and verification as physical layouts must be RET compliant and conform to the mask fabrication rules. In the low K1 area, marked as RET dominated in Figure 1, more complex design flow has to be implemented. (Figure 3) This more complex flow creates RET-imposed distortions of the design shapes based on models of the mask writing and lithographic processes. By basing RET corrections on calibrated models of mask and fabrication, one can substantially compensate for the

insufficient transfer function and manufacturing margins of the low contrast lithographic system. Unfortunately, this flow does not guarantee adequately accurate replication of the design shapes to guarantee success. The fabricated thin film pattern distortions may create shorts and opens (yield issues), electromigration hot spots (reliability issues), or changes in electrical parasitics that fatally impact electrical functionality. Consequently, as is the case with electrical function-based design automation, verification of the result is essential to productizing the design. In this flow, verification is either accomplished by a full chip simulation tool or by measuring the actual silicon result. This methodology requires advanced EDA tools in order to overcome yield and signal integrity issues.

Post-RET

The complexities in mask data and manufacturing make it highly desirable to verify and optimize the mask data independently before committing to the costly fabrication process. An effective method for post-RET mask data verification is to simulate its image on the silicon wafer and compare it with the original design intent. This method places mask data in its intended operating environment and evaluate its performance metrics that have direct impact on wafer imaging. A simulation based verification system can evaluate the process for a product and give warning on certain performance limiting spots on the layout and thus significantly reduce the risk of mask data errors. Once the troubling spots are identified, localized corrections can be applied to extend the process window in an intelligent way.

The existing model based mask layout verification systems have a few areas that require further improvement. First, they are typically implemented with the same simulation engine with model based OPC. Sharing the simulation engine with OPC, the verification also inherits the errors of the OPC model. The logical dependency jeopardizes the probability of finding OPC errors, and reduces the reliability of the verification. A process window is the range of process parameter variations under which the line width remains within limits Secondly; they employ empirical modeling approaches that cannot easily track acceptable variations in process conditions. In order to sample a different condition in the process window, a different set of models has to be developed, which consumes significant effort and time.
In addition, there is no inherent reason why one set empirical models can judge the result of another if they are derived from the same set of mathematical formulation and training patterns. A full-featured photolithography simulator for mask data verification has been developed for the past decade by the major EDA vendors. (Mentor Graphics, Cadence) These types of simulators have been used extensively in lithography process development where they have demonstrated high accuracy for process predictions.
A mask data verification flow around the physical lithography simulation core that is independent from the OPC engine, thus free from the logical dependency between OPC and its verification. The use of physical models opens the possibility for achieving higher prediction accuracy on complex layout configurations. In addition, physical model can naturally predict the pattern transfer behavior under process variations such as focus change. Furthermore, a physical layout design can efficiently leverage this physical model simulator to improve circuit performance and reduce the manufacturing variations.

Another consequence of MDP methodology is that design rules no longer guarantee robust manufacturing of the IC design, which is the classic, and simple, assumption that has permitted implementation of economic models such as those in which a fabless company sends designs to a foundry and achieves one-pass success.

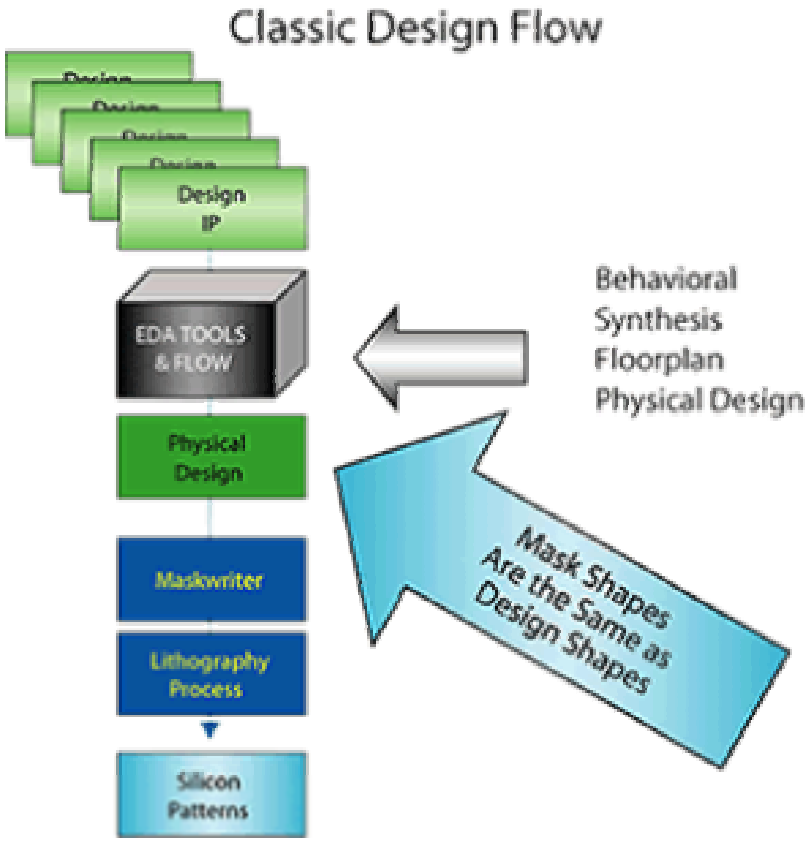


Figure 2 -Classic design and MDP flow
Source: Montgomery Research

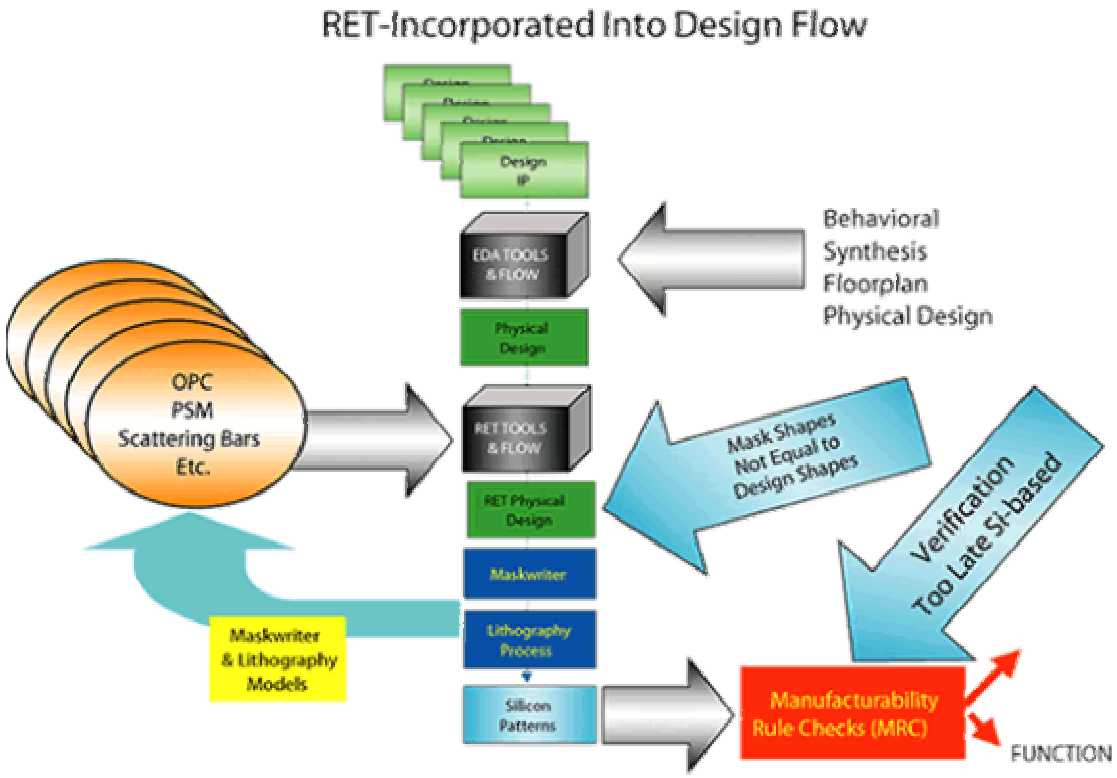


Figure 3 – RET incorporation into the Design Flow
Source: Montgomery Research

One-Pass Low-K1 Success: RET-Driven Design

One-Pass successful design is the way that the industry is aiming towards. In this strategy, the building blocks of the design are optimized for sub-wavelength fabrication before the large-scale, full-chip integration of these blocks occurs. Figure 4 shows one way in which the design paradigm can be fundamentally changed to guarantee fabrication robustness. On the left side of Figure 4 is an optimization loop in which circuit blocks are put through a virtual manufacturing flow to certify them for manufacturability. These blocks are usually pre-designated (design IP) and can come from many sources. These can be internal to the company creating the design as well as external, e.g. schematics or physical blocks for industry standard busses, communications RF/analog/mixed signal blocks, etc. In this flow, the design IP is brought to the physical design (for example, GDSII) file format. This block is then pushed through the RET tools flow, and the resulting RET-modified design is modeled

in a virtual mask-writer, with new distortions peculiar to the write tool and process of the target mask shop. The 'virtual mask' shapes are then transformed by a model of the stepper imaging, resist development, and pattern transfer processes to create 'virtual silicon patterns.' These can be inspected for physical yield integrity (lack of shorting hazards, lack of unacceptable necking, etc.). They can also, especially in the case of electrical parasitic-sensitive blocks, be checked for electrical function integrity. For example, the 'RET tools and flow' block in Figure 4 should add dummy features, or 'tiles.' The function checker will then simulate the electrical effects of these new features on circuit function.

If there are yield or function issues, the re-design path of Figure 4 is executed and fixes the block well before designers begin integrating it into a full-chip design.

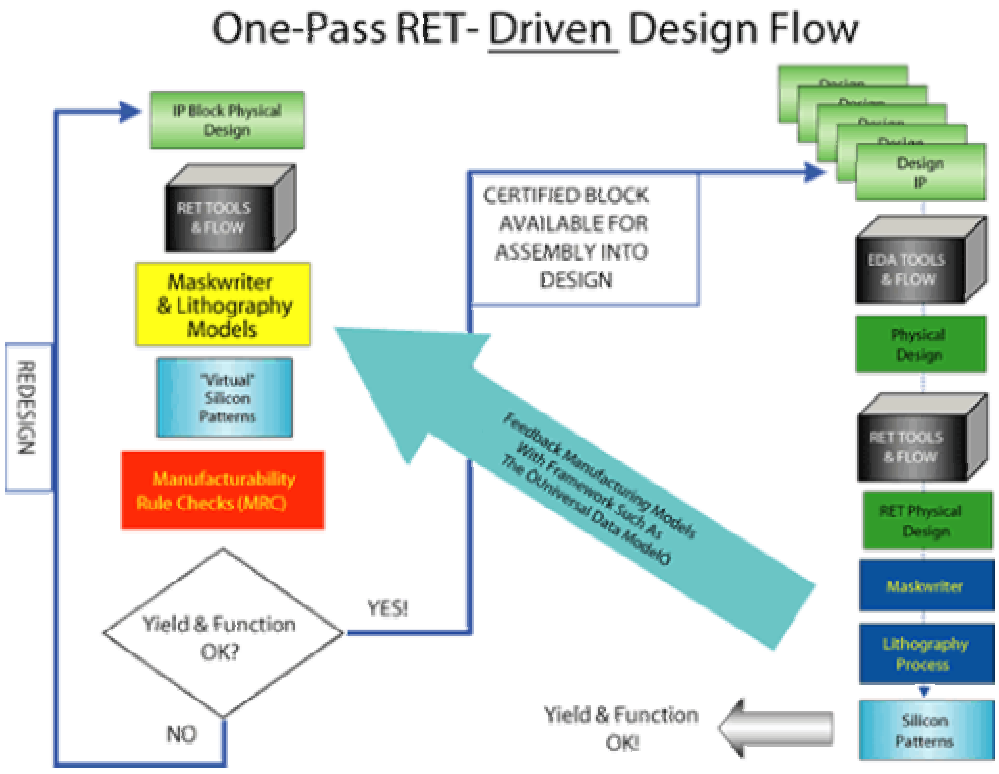


Figure 4 –One-Pass RET Driven Design Flow
Source: Montgomery Research

This is a predictive engineering strategy of great power and deals in a fundamental way with the issues resulting from the fact that design is not equal to the silicon image. It fixes the consequent physical yield and circuit electrical parasitic failures at the design block level. It is critical that this flow not only be exercised to fix nominal problems, but also to correct for statistical ones relative to manufacturing tolerances. This latter point is very important. Sub-wavelength issues are significant at nominal exposure conditions, but even more significantly increase risk of failure as focus or

exposure deviate from nominal in actual manufacturing. Consequently, statistical verification is a must.

When the true full chip integration and fabrication is implemented, as is described on the right side of Figure 4, the silicon image result is much more likely to be free of fundamental block-level issues. Remaining full-chip integration specific issues may be discovered at this stage, but they are as likely to be the classical ones that designers and tools address, namely architectural or full-chip timing and power verification issues rather than sub-wavelength distortion effects.

Silicon simulation

Silicon simulation is the capability to predict the pattern printed on silicon for a given layout. This is a complex task, as there are many factors in IC manufacturing that influence a silicon image, including original layout, mask process, stepper optics, photoresist characteristics, and develop and etch steps. Silicon simulation takes into account the impact of all these steps and characteristics on layout, and produces a simulated printed pattern that predicts what the layout would look like in silicon, without having to go through the costly and time-consuming manufacturing process.

One of the applications using silicon simulation is silicon vs. layout verification, which uses simulation to compare the silicon "image" against the ideal "drawn" layout. Due to the nature of sub-wavelength issues, the last step in every sub-wavelength design must be silicon vs. layout verification.

Today, there are several valid "insertion points" for applying OPC. Most designers apply OPC at the end of the design cycle, once the design is entirely completed. This allows the OPC process for each geometry to take the proximity effects from all neighboring geometries into account and correct accordingly. Nevertheless, there are other design practices where OPC is embedded in the SoC IP (such as standard-cell libraries) or in the bit cells of embedded memories in order to ensure high manufacturing yield or performance tuning. It is also very conceivable that OPC may be done at different points during the design flow, depending on the nature of the block.

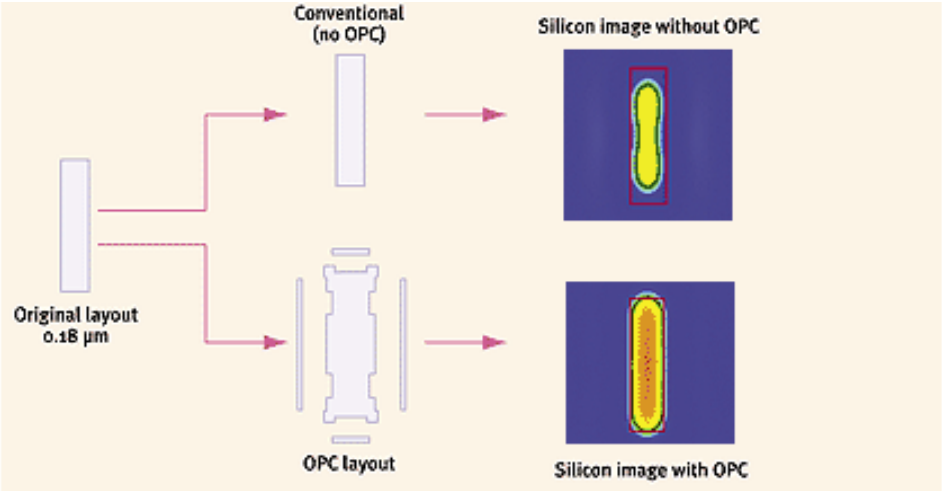
Sub-wavelength design methodologies and tools provide OPC capability in many different points during design flow, including at library creation; at custom-block creation; during integration of blocks; at physical verification; and during mask data preparation. Also, these tools support different styles of OPC as automatic vs. manual, rules-based, model-based and hybrid, and simple vs. aggressive corrections. These tools are flexible for integration of portions with different types and levels of OPC. Only through this flexible design methodology can the optimal level of OPC be applied to meet the performance, manufacturing-yield and mask-manufacturing requirements of the design.

Phase aware physical design requires a physical-design environment (consisting of methodology and tools) that handles phase conflicts on a global and local scale, on the fly and in a transparent manner. The goal of phase aware design is to produce layouts that do not have any phase conflicts, and therefore guarantee success in manufacturing the corresponding mask set.

To that end, a phase aware physical-design tool must first detect possible phase conflicts that exist in the layout and transparently resolve them. By the same token, if an operation in any of these phase aware tools were to cause a phase conflict anywhere in the layout, the conflict would automatically be identified and avoided.

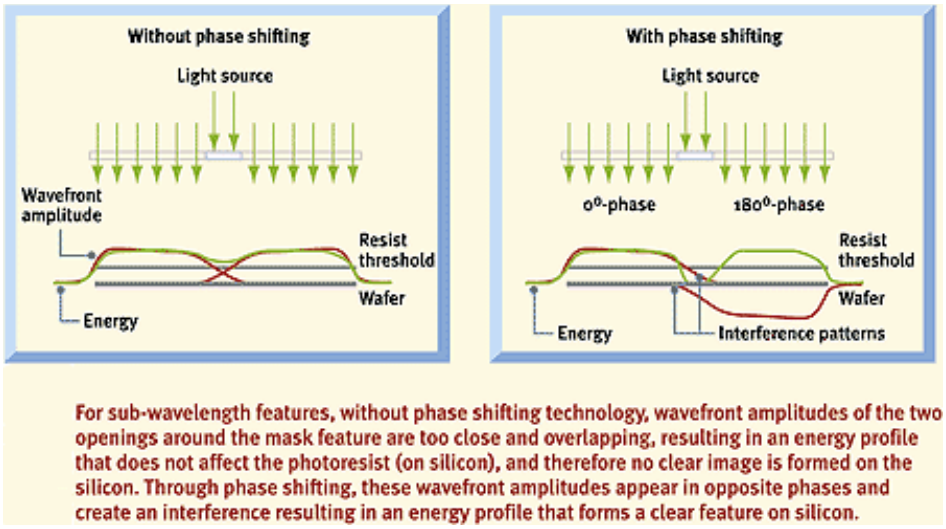
Furthermore, since physical design tools also take timing into consideration (such as timing-driven placement), phase aware physical design tools must also take into account the effects of phase shifting on timing whenever applicable.

Major EDA vendors offer advanced tools for OPC and PSM. These are a 'must have' factors for manufacturing. Yet, as we are getting into 65 nm and below these methodologies need to be significantly modified in order to keep accurate manufacturing.



Optical proximity correction (OPC) is a corrective technique that adds small objects to a photomask that will not print frequently by enlarging corners or adding bias lines to the edge of a feature.

Image Source: EEDesign



For sub-wavelength features, without phase shifting technology, wavefront amplitudes of the two openings around the mask feature are too close and overlapping, resulting in an energy profile that does not affect the photoresist (on silicon), and therefore no clear image is formed on the silicon. Through phase shifting, these wavefront amplitudes appear in opposite phases and create an interference resulting in an energy profile that forms a clear feature on silicon.

Image Source: EEDesign

Implications for Design Tools and the Role of a Standard Data Model

Figure 4 describes a 'should be' model for sub-wavelength design, one for which not all the tools and modeling methods are available today. Figure 3 shows that manufacturing tools for both masks and wafers must be characterized so that appropriate models of the manufacturing process can drive accurate physical and electrical simulation of mask and wafer fabrication. The EDA industry is beginning to create the verification tools to implement this flow, but today these tools are a partial toolkit of somewhat primitive tools.

For significant progress with the strategy described here, these tools will need to be refined in accuracy and efficiency. They will require as inputs information from manufacturing that ideally should be described in an open industry standard. Such a standard constitutes a design for manufacturability data model for a manufacturing-aware design framework. One such standards activity that fits this description is the currently designated "universal data model" (UDM) initiative sponsored by SPIE and SI2. This initiative aims as one of its goals to supply the "manufacturing models" feedback loops shown in Figure 3 and Figure 4. The initiative has several desirable attributes. It will produce an abstract description of the properties of data objects and the behaviors associated with them – an object-oriented paradigm. While the description will be an open standard, the implementation can be open (e.g., in OpenAccess) or proprietary (e.g., an extension of Synopsys' "Milky Way" framework). A goal of the UDM initiative should be to create objects that describe the behavior of fabrication processes so that the tool behaviors can be driven by easily represented "reduced models" of the tools and processes.

Succeeding in this goal may help recover some of the logistical practices that drive today's semiconductor industry. No longer can a foundry or fab drive successful design by simply supplying a design-rules deck to designers in an IDM or fabless design company. But a successful UDM-like activity, along with the flows in Figure 4, can permit a more complex set of model decks to permit manufacturing reality to drive the design process. Accomplishing this goal will have achieved the holy grail of today's industry visions of design for manufacturability.

Conclusion

In order to achieve successfully nanometer-scale designs to market, semiconductor companies must address a growing array of challenges—from ever-more stringent design rules to increasing chip layout complexity. IC's designers must also contend with the physical effects that become much more troublesome at these smaller geometries. A new standard emerged called: Design for Manufacturing (DFM). Complex combinations of voltage drop, signal cross-coupling and circuit parasitics interact to stretch design cycles and force re-spins. Process variations across the die, wafer, and batch affect yield, performance, and reliability. In addition, burgeoning volumes of parasitic data strain storage facilities and choke chip analysis software.

Currently, major EDA vendors provide comprehensive Design for Manufacturing (DFM) solutions by addressing the two key aspects of the design flow, physical verification and sign-off electrical verification. Both enable a reliable way to achieve manufacturing sign-off before tape-out. Yet, as we step down into lower nanometer range, current tools and methodologies may not provide accurate DFM solutions. It is a constant race to achieve an efficient, on time nanometer design.

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