Nanometer Physical Verification

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Abstract

In today's competitive marketplace, designers of leading-edge integrated circuit face constant pressure to deliver first-time working silicon within tight schedules. As we are stepping into the nanometer era, IC's complexity is increasing, die areas are also getting larger in order to incorporate the increased functionality that comes with more advanced technology. The end result for physical verification is that larger layout databases need to be checked, with an increased number of more complex rules in the same ambitious project time frames as before. At 90 nanometers and below designs that pass physical verification such as design rule checking (DRC) and layout vs. schematic (LVS), may not function as expected due to additional electrical side effects inherent in nanometer process technology. Therefore, nanometer designs require additional verification before being approved for tape-out. If signal integrity (SI) and other electrical effects are not considered, a design will likely suffer from lower performance, lower yield, and consequently functional failure. Any failure identified after the design is manufactured will result in expensive mask changes and delays in getting the IC to market. This article highlights some of the industry problems associated with verifying nanometer ICs and discusses some of the current industry's standard verification tools and their capabilities.

Introduction

Implementing nanometer-scale ICs raises significant SI (Signal Integrity) related issues that have to be verified in order to avoid chip functional failure. These include reduced feature sizes, decreases in wire pitch, lower power supply voltages, and shrinking threshold voltages. With each new process technology, more and more levels of wire are packed more closely together. As a consequence, the fraction of total wire capacitance represented by lateral coupling increases dramatically. This in turn is responsible for a dramatic increase in on-chip crosstalk noise. Another electrical problem in nanometer designs is increased clock frequencies with faster on-chip slew rates. Faster slew rates create more switching noise and increase instantaneous power consumption. This in turn puts stress on the power grid, resulting in voltage (IR) drop and electro-migration. Nanometer sign-off is becoming a challenge, uncovering any problems that may have been missed during design implementation or that have been caused by last-minute manual design changes. Nanometer sign-off is a final verification to assure that a design does not have electrical issues that will result in chip failure after manufacture. However, finding many problems only just before tape-out could lead to multiple design iterations and missed schedules.

The tools used during design implementation to support design closure should be fast and flexible in order to maintain design productivity. These tools should guide the design's electrical integrity continuously, without major compromises to design performance, power, or area. The final sign-off phase requires an integrated tool suite that is production-proven and validated against real silicon. Nanometer sign-off tools used during this phase should be more thorough and accurate than the design closure tools used during implementation. Full-chip examination should include analysis of the subtle and complex interactions that occur between many different electrical effects across many process corners. Nanometer sign-off should predict how IR drop affects crosstalk—and how this affects timing, which in turn affects power, which is responsible for IR drop. Another key component of nanometer sign-off is accurate 3-D parasitic extraction, full-chip IR drop analysis, full-chip crosstalk analysis, and SI-aware static timing analysis (STA) that accounts for the influence of both crosstalk and IR drop.

EDA vendors are constantly improving their tools in order to provide full coverage for nanometer technology. Although current commercial EDA tools provide successful solutions, yet not all types of designs can be verified efficiently. Especially when dealing with massive data volumes associated with large nanometer designs. As a result, designers are relying on in-house DA and programming in order to achieve acceptable results, often taping out in full knowledge of the risk that latent nanometer-related issues remain undiscovered.

Nanometer Electrical Effects

1. Design size and complexity

One of the major issues of nanometer designs is their size. At 0.18 micron, there are designs with over 250 million transistors. Nanometer designs support multiple-billion transistors within the next few years with no corresponding relaxation of time-to-market demands. Implementing these designs require nine or more layers of metal, multiple metal pitches, via densities measured in millions per square centimeter, and pervasive use of flip-chip packaging to distribute thousands of I/O pins. These advances create three related issues designers must address-capacity and performance; early, accurate analysis; and hierarchy to manage complexity. A nanometer design environment must have the capacity and performance to handle these huge chips while imposing as few methodology restrictions as possible. Verification tools for DRC, LVS and SI have to process very large database in fairly fast time! For the past few years many attempts were made to create faster verification tools to shrink process time.

2. Delay Behavior

Delay behavioral is probably one of the most significant issues. In addition to dominating overall delay, nanometer design exacerbates physical effects that introduce substantial delay-notably signal integrity (SI) and IR (voltage) drop. These effects can be considerable even at 0.18 micron. By 0.13 micron, "sign-off" timing analysis tools miss numerous SI- and IR drop-based degradations that are comparable in magnitude to the nominal timing and much more difficult to predict. Yet, many design teams continue to use delay calculations based on over-simplified models (such as lumped capacitance) down to 0.13 micron. Doing so results in both

reduced performance-due to high margins-and excessive, time-consuming design iterations. At 90 nm and below, timing analysis that does not include SI and IR drop effects is essentially meaningless.

3. Cross Coupling

Delay is a function of wire loading and wire drive. At 0.25 micron and above, the primary wire capacitance is due to coupling to electrical ground and is largely proportionate to wire length; doubling the wire length doubles the capacitance. Steiner, or global, routing estimates predict the wire length based on placement.

As process geometries decrease, the primary capacitive coupling on a given wire moves to its neighboring wires. Capacitance depends on the local wire geometry and, in many cases, to the actual signals on neighboring wires. As an example, Figure 2 shows delay variation at 0.18 micron due to capacitive coupling for signals at 1X and 2X grid spacing. The variation is up to +/-30% for 1 mm wires and +80%/-60% for 3 mm wires. At 0.18 micron, cross coupling affects only high-performance designs significantly. At 90 nm and below, it significantly affect all designs. Since capacitance is no longer strictly proportional to wire length at nanometer geometries, detailed routing is required for accurate timing analysis.

4. IR Drop

Resistance in the power and ground wire networks creates IR drop. Nanometer designs are extremely susceptible to these effects because this resistance increases with decreasing feature sizes. It is further exacerbated when the overall power supply voltage decreases because this also decreases the usable region of the signal transitions. With decreasing supply voltage, gate delays and noise susceptibility increase. An IR drop from 1.7V to 1.6V is capable of producing delay variations of 50% or more. One study of designs at 0.18 micron and below showed that 20% of designs failed on first silicon due to excessive IR drop alone. As process shrinks below 90 nm, IR Drop issues can cause major failure in the IC functionality.

5. Manufacturing Verification

Above 0.13 micron, manufacturing procedures such as optical proximity correction (OPC) were performed after generating the fully routed, and otherwise correct, GDSII. Design teams could also ignore the effects of physical manufacturing processes.

Most design teams run into manufacturability issues for the first time at 0.13 micron. Processes using copper wiring, chemical-mechanical polishing (CMP), and sub-wavelength lithography lead to exceedingly complex and arcane design rules. Antenna rules, to take one example, require careful handling to avoid via proliferation and minimize wire lengths. Furthermore, foundries continue to change the design rules long after the introduction of a new process in order to optimize time-to-silicon production.

Nanometer routers must explicitly provide for variable width and variable spacing, and they must be capable of adapting to the requirements of copper, multiple vias, OPC, phase-shift masking (PSM), and CMP. Beyond 90 nm, routers have to optimize the wiring specifically to facilitate manufacturing processes. Nanometer designs challenge any router that is not designed specifically to account for these advanced process considerations. The industry's standard verifications tools provide a successful solution for this issue yet as we step down to 65 nm and below manufacturing challenges arise.

6. Massive routing capacity and performance

A nano-router must take into considerations SI issues on-the-fly. At 0.13 micron and above, design teams can perform routing block-by-block, then use a chip-level router to connect the blocks together and perform tasks such as generating the top-level clock tree. Nanometer routers must be capable of working simultaneously at the block-level and chip-level.

The router must be tightly coupled with, and have control over, almost every aspect of the physical realization of the chip, including:

- Routing-optimized placement
- Local logic optimization for timing fixes and area recovery
- Clock tree construction and balancing, including useful skew
- Power grid construction based on IR drop and EM analysis

Nanometer routers must have concurrent access to full parasitic extraction, full-chip static timing analysis (STA), and signal integrity analysis, using these results to guide and to modify routes on-the-fly. High-end design teams must account for the complex interactions between signal, power, and clock routing. For instance, in 90 nm high-performance designs high-speed clock routing must be tightly controlled using techniques such as shielding, track assignment, and topology control. Routing must be integrated with automatic clock tree synthesis and clock timing analysis.

Performing the above, along with supporting variable wire widths and spacing, requires massive capacity and performance. A meaningful benchmark is the ability to route a 100M gate design overnight. Doing so is likely to require multithreading and multiprocessing in order to utilize all computational resources available for the task. As process shrinks below 90 nm new rules have to be followed. Comprehensive routing analysis is essential for functional verification.

7. Reliability Verification (RV)

At nanometer levels, the layout view does not reflect the actual resulting silicon. An actual simulator is needed in order to estimate the end result silicon. Wire widths change due to optical distortions from sub-wavelength lithography. Wire thicknesses change due to CMP on copper wires, producing effects such as erosion and dishing. Such distortions substantially affect electrical characteristics-capacitance, resistance, and inductance-and reliability-EM-in signal wires, clock, and the power grid. Design teams need analysis information that reflects these realities.

With the right analysis information, design teams can also get significantly more performance out of a given process technology. Microprocessor design teams using full-custom techniques often achieve 7x to 10x higher frequencies at given process nodes than typical ASIC design teams using semi-custom techniques. A considerable part of the difference is based on having accurate physical analysis information, which enables designers to cut margins tremendously. As a result, they can gain performance at a given process node or reduce the cost per chip by using a less expensive process node. EDA vendors provide tools that can successfully provide a simulation of the actual silicon and predict manufacturability failures. Still, as process goes below 65 nm not all phenomenon are detected, leading to functionality failures.

8. Parasitic Extraction

Extraction accuracy is essential. Accuracy is largely a function of the relationship between the tool vendor and the foundry. Tool vendors need early access to proprietary process information to determine how best to model the process and to capture the necessary process characteristics. Accuracy is also a function of the design representation. Tools need to use the physical details of design elements, rather than simplistic abstractions. As an example, while it is expedient to provide a simplified model of a port, doing so inherently limits design optimization. Similarly, cell models should be instance-specific, not treated as if each cell were isolated.

From a methodology point of view, getting the most out of the silicon requires utilizing the most accurate physical information necessary during every design iteration. During early design iterations, turnaround time is at a premium. Later in the design cycle, accuracy is most critical. Using a less accurate extractor to speed iterations can mean increased margin and increased timing closure risk. An extractor should be fast enough to enable designers to complete block iterations within 1-2 hours. It should also complete a full-chip extraction overnight, using multiprocessor computers if necessary to do so.

9. Delay Calculation

Delay calculations performed by today's "sign-off" timing analyzers are inaccurate. These tools often use over-simplified models (such as lumped capacitance) that do not take into consideration dynamic effects on the wires, which in turn have dynamic effects on cell delays. Cell delays change with loading on the gate as well as with coupling effects on nets. The delays are dynamic, not fixed. To be accurate, delay calculation must be based on more than a behavioral abstraction of the cell. It must take current and capacitance characteristics into consideration, down to the transistor level. Cell delay calculation based on lumped capacitance simply is not accurate enough for high-frequency circuits. Nanometer delay calculation must be based on SI and IR drop. Hierarchical delay calculation is also important in nanometer design. Simplistic, conservative timing models at hierarchical boundaries increase margins. Delay calculations must correctly model paths that cross hierarchical boundaries to maintain accuracy.

10. Electro-Migration

Signal EM becomes more of a problem as wires get smaller and designers are forced to push more current through them to meet performance. Place-and-route tools that create large drivers on nets to meet timing can create EM problems throughout massive chip-problems that design teams do not even know about. Nanometer physical verification must identify EM problems before they occur in silicon, including AC-induced EM due to high-frequency signals-generally those over 300 MHz and those with many hazard-as well as DC-induced EM due to large unidirectional current flow.

11. Power Grid analysis

Power grids account for approximately two-thirds of all wires. In nanometer designs, they contain over 1 billion wire segments (resistors). As opposed to signal nets, which are generally considered one at a time, power grids must be analyzed in their entirety, making tool capacity important and hierarchy support crucial. Power grid analysis must include IR drop and EM analysis. Using over-simplified models to accelerate IR drop analysis can be an extremely expensive shortcut when the silicon fails due to EM.

Accurate power-grid analysis requires modeling design activity that is representative of the actual signal transitions. It is getting extremely difficult to provide adequate vector sets for many complex designs. Power-grid analysis tools should be able to use probabilistic techniques which can provide accuracy that neither static methods nor vector-based methods can match for a growing number of designs. For accuracy, power-grid analysis must also take into consideration manufacturing techniques such as OPC and PSM, necessitating the ongoing model calibration to foundry silicon.

12. Inductance

Specialized solutions focused on extraction exist today for large circuits. While vendors are introducing specialized capabilities for very larger designs, complete solutions are unlikely in the near term. One major challenge in extracting and analyzing inductance is that doing so can be extraordinarily computationally expensive, requiring perhaps an order of magnitude more computation than cross-coupling analysis for the most detailed solutions. Continuous convergence can help design teams identify the wires that are most susceptible to inductance problems, so they can utilize such computationally intensive tools beneficially.

13. Massive database capacity and performance

Nanometer databases should provide a 100x capacity improvement over the previous generation of physical design databases without degrading performance. In fact, performance on operations such as read and write need to get significantly faster. Transparent support for 32-bit and 64-bit versions of popular processors and operating systems is also important. Most designers prefer using 32-bit machines. Transportability enables them to do so for design representations within the memory limit. Designers who need to use applications beyond the 4GB limit should be able to do so without the entire design team having to move to 64-bit machines.

High database performance enables many tools to operate directly off the database, saving application development time. While some tools are using their own proprietary data structures for runtime efficiency, the persistent repository remains the centralized database. If the database also has an appropriate extensibility model, fewer and fewer applications will duplicate structures, such as the netlist, that already exist in the database.

14. Extensibility

It is impossible to predict all future design information requirements, so nanometer databases should support the creation of new object types, the addition of attributes to existing objects, and the definition of new relationships among objects-all with native speed and efficiency. Such extensions must be lightweight, space-efficient, time-efficient, and optimized for the particular data type.

With appropriate extensibility, application developers-including in-house and third-party tool developer-can write efficient algorithms to manipulate and analyze the data they need precisely at full speed. Extensions should be available permanently to enable other tools to use them, or temporarily to serve as a coherent high-performance cache. In-memory coherence makes it possible to write tools built from cooperating components that are incremental in nature, to use lazy evaluation techniques, and to provide application-level toolkits that allow rapid new tool evolution and construction.

Nanometer databases should be open, which includes having an open application programming interface (API), open source code, and a community-based oversight committee. Openness is not a technical requirement, but it directly facilitates a technically superior implementation that advances rapidly. It also mitigates design team risk by enabling native third-party and in-house application development.

Current Industry's Standards

Major EDA vendors are providing a wide range of verification tools. One of the leaders is Calibre from Mentor Graphics. Calibre Physical Verification and Sub-wavelength Manufacturability Tools suite is one of the industry's complete physical verification and sub-wavelength solution. Calibre physical verification tool suite, which includes Calibre DRC and Calibre LVS, ensures that IC physical designs conform to manufacturing rules and match the intended functionality of the chip. As the market leader in physical verification tools, Calibre is the industry standard, used in 19 of the world's 25 largest integrated device manufacturers, as well as all the top foundries and deep submicron library providers.

For sub-wavelength designs, Calibre leverages its hierarchical verification engine to provide a tool suite to add, model and verify layouts for all four RET techniques: optical & process correction (OPC), phase-shift mask (PSM), Scattering Bars (SB) and off-axis illumination (OAI), plus the new techniques such as sub-100-nm capable double-exposure dipole decomposition technique currently being refined for production deployment.

Cadence is offering an entire set of tools to cover many aspects of nanometer design verification. Among these tools are NanoEncounter, place & Route and NanoRoute Ultra independent nanometer router. Cadence also offers EDA tools for signal

integrity, delay issues, power integrity design/analysis and physical verification for nanometer design.

Synopsys offers also full nanometer design support in a variety of EDA tools. For example part of the Galaxy Design suite is Hercules PVS. Hercules PVS includes full hierarchical processing and utilizes a combination of distributed processing and multi-threading capabilities to offer users unsurpassed verification speed. Hercules is tightly integrated within Synopsys' Galaxy Design and DFM tools including Astro place and route software, Star-RCXT parasitic extraction software and SiVL lithography verification software. Since Synopsys' Galaxy design tools are based on the Milkyway common database, these tool results are easily read into Hercules to perform DRC, ERC, and LVS. With all tools sharing a single common database, time-consuming data translation steps, the risk of translation errors, and the headache of database incompatibilities are eliminated.

Conclusions

Successful nanometer physical IC verification requires advanced tools and methodologies in order to cover all nanometer effects. Nanometer success also requires a new set of implementation, analysis, and database technologies.

Silicon integrity and IR drop have become first-order timing effects, and EM is an issue for signals as well as the power grid. An extensible, unified database provides the foundation for nanometer design, especially since most designs are be digital/mixed-signal. It needs to support a rich set of objects, attributes, and relationships. Perhaps more importantly, it must support extensibility with native performance. The database and all nanometer tools should support hierarchy elegantly and handle 100M gate designs efficiently.

No Doubt, nanometer design implementation places extraordinary demands on design teams. Those that embrace wire-centric design strategies such as continuous convergence will thrive at the expense of those that do not.