Performance Limitations of Nanometer Physical Verification

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Abstract

Increasing complexity and integration, shrinking geometries and consequent physical effects have been some of the ongoing challenges of the nanometer era. The importance of first-pass silicon is a critical requirement in our today's IC design market. Each advancement in process technology results larger numbers of process layers and transistors, requiring more design and manufacturing rule checks before manufacturing handoff. This results dramatic increase in physical verification runtime and increase in violations analysis, threatening tape-outs deadlines and time to market. The size and complexity of modern designs add another crucial challenge to the current physical design verification technology. Designers need more effective and fast physical verification capabilities in order to deliver accurate results required to keep projects on track. The daunting cost of mask sets for nanometer processes creates additional pressure to detect and correct errors as early as possible in the physical-verification process. Longer physical-verification cycles can delay time-to-market, but incomplete rule checking can reduce yield, degrade reliability, and invalidate functionality. The combination of complex rules, more transistors, and extra levels of wiring presents a formidable challenge to today's physical-verification tools.
In this paper I will describe nanometer physical verification on-going challenges. I will discuss design performance challenges, EDA industry's approaches and roadmap to provide efficient solutions.

Introduction

Designers can no longer rely on the typical physical verification methods to deal effectively with the complex rule decks and massive data sets associated with today's nanometer designs. EDA companies are constantly presenting with newer concepts to physical verification attacking new set of constraints and requirements, delivering capabilities that reduce violations correction time for today's increasing designs. These new verification methods are aimed for 'look ahead' concept, trying to save significant design time, causing resources saving, while also provide rules simplifications. Although EDA technologies are rapidly 'chasing' nanometer technology it does not provide an entire set of solutions. Corporations are enforced to develop on-house methods, concepts and even software in order to find compromising solutions to their deep nanometer issues. Accuracy is insufficient. Today's physical verification methods force engineers to work via long design verification process before detecting design violations information. This delays development cycle, forces additional iteration cycles, and worse of all

tape-out schedules! As design is scheduled to tape-out at a certain date but has to pass final verifications (For example: Reliability), the chance of last minute corrections is very high and may results tape-out delay of days up to weeks. (Depend of type of potential violations that have to be fixed.) The new trend of verification solutions deliver design violations information embedded into the design stage and debug environment concurrently with the physical verification process. In a way it is some sort of predicted information to accelerate violation correction time and reduces the number of repeated cycles. Beside more efficient design analysis the new methods are focused on performance increase which significantly reduces the duration of verification iterations, speeding the development of nanometer designs. EDA vendors are constantly working in these two major arenas, effectiveness and speed!

Limitations of today's Verification Methods

- **General**

Today's physical verification methods face an increasing set of challenges to their ability to maintain speed and results accuracy for nanometer designs. New nanometer manufacturing phenomenons that are associated with dense geometries, and packed interconnect creating an information overflow for our current verification methodologies. Rule decks design and preparations have become almost impossible without programming automation. With earlier process technologies, DA engineers were able to rely on fairly simple combinations of primitive commands to build comprehensive rule decks. Typical rule decks for design-rule checking (DRC) for tools like Dracula, DIVA, Hercules could be construct and tested within reasonable time frame. The complexity of design rules were simple to moderate and the task of filling specific requirements for physical placement, spacing, and enclosure, could be done within few days. With today's nanometer process requirements, designers are forced to combine increasingly long and convoluted sequences of primitive commands to address complex, yet common verification situations. With each new technology the number of physical design combination increases almost exponentially and a single check might contribute hundreds of lines to the rule deck. New process rule deck may include thousands of lines and can not be done within reasonable DA time without the usage of automation. Creating and debugging rule decks become complicate task and consume significant time. Another major problem is the potential of creating faulty design rules. A sequence of primitive rules, assembled together, generally only approximates the designer's intention for more complex checks, reducing results accuracy at a time when greater detail is necessary to uncover potential design faults.

- **Rule Deck Processing**

Processing rule decks, today's methods and tools are facing serious runtime issues. Typical verification tool distributes processes according to rule and layer which results an un-even task sizes. Recurrence of a small number of commands, performing on one or two layers (for example sizing or enclosure) determines the minimum runtime for the entire deck. This is a direct result of conventional multiprocessing scheme that cannot further decompose these types of commands. Comparing to all other tasks that individually occupy only a short time of CPU time each, these `show stopper' command sets that take many hours to complete delay delivery of the final results to the waiting design team. It does not matter how fast the rest of the verification goes. If the system is delayed beyond reasonable limits due to `show stopper' commands the end result will be delivered significantly delayed, regardless of how quickly it was able to complete the rest of the job. The traditional parallel processing based verification methods are no longer providing the best solutions. Nanometer rule decks require a greater effort designing checks that are derived from design and manufacturing limitations. What we call, the halo effect (Zone of influence that encompasses neighboring structures) has become more common, affecting more structures and further limiting the efficiency of multi-processing execution. The common verification checks are also becoming complicate due to the combination of primitive inefficiencies and growing halo effects. This adds another delay factor to the entire run. As process technology progresses we are witnessing increasing inaccuracy and efficiency providing physical verification, using our current methods.

- **Hierarchical Processing**

Beginning in the late 1990s, physical-verification EDA tools began to implement hierarchical pre-processing as a means to manage the increasing complexity of design-rule checks (DRCs). In such a methodology, a hierarchical pre-processor identifies repeated patterns of cells and polygons in the design. The pre-processor artificially creates a new level of hierarchy around each repeated pattern, so that the DRC tool checks each pattern only once rather than every time it appears in the design.

The emergence of complex nanometer designs introduced new verification challenges. The lithographic limitations of today's manufacturing processes increased the effective interaction distances between polygons in the design (the so-called "halo effect"). These designs are using larger amount of cells and in different shapes, which results a greater number of permutations and combinations of abutted cells. Abutting cells cannot be hierarchically partitioned and this limits partitioning opportunities in the overall global design. This dramatically reduces partitioning opportunities and, therefore, negates much of the effectiveness of hierarchical pre-processing. Although

the benefits of a well-planned hierarchical design remain indisputable, new halo-based rules claim a growing proportion of physical-verification runtime. The fact is that the hierarchical approach of the current generation of DRC tools will cease to have any significant benefit at the 65-nm process and below. The way out is to perform what we call a 'virtual flattening'. The flattening of large nanometer designs, including its complex design rule is virtually going back to the dark ages from technology and efforts perspectives. Physical design verification may takes days or even more and it is definitely not within reasonable design time limits. No Doubt, hierarchical verification approach is no longer the ultimate answer for today's verification obstacles. There is a need for a new direction in order to improve the performance and accuracy of today's physical verification.

- **Parallel Processing**

In mid 90's, the massively parallel approaches to physical verification boost throughput to the point where design teams can meet schedule requirements and, simultaneously, address subtle nanometer manufacturing issues that significantly impact yield. Designers could enhance the scope of manufacturing checks but stay on schedule. In addition, these systems delivered an earlier, deeper, more accurate assessment of the impact of design decisions on yield in nanometer process technologies. Today's physical verification tools are unable to effectively utilize popular Linux-based servers due to the fact of their rule-based multiprocessing models that cannot overcome the long poles in the rule deck. As a direct result the performance curve flattens dramatically after 6-8 CPUs leads long physical verification runs even on large and expensive parallel processing systems. Again we are witnessing the inefficiency of a concept that provided us great solutions about a decade ago. The industry demands a new approach to the parallel processing method. A new approach that will incorporate few methods with an effective usage of parallel processing, in order to successfully achieve accuracy and speed in nanometer physical verification.

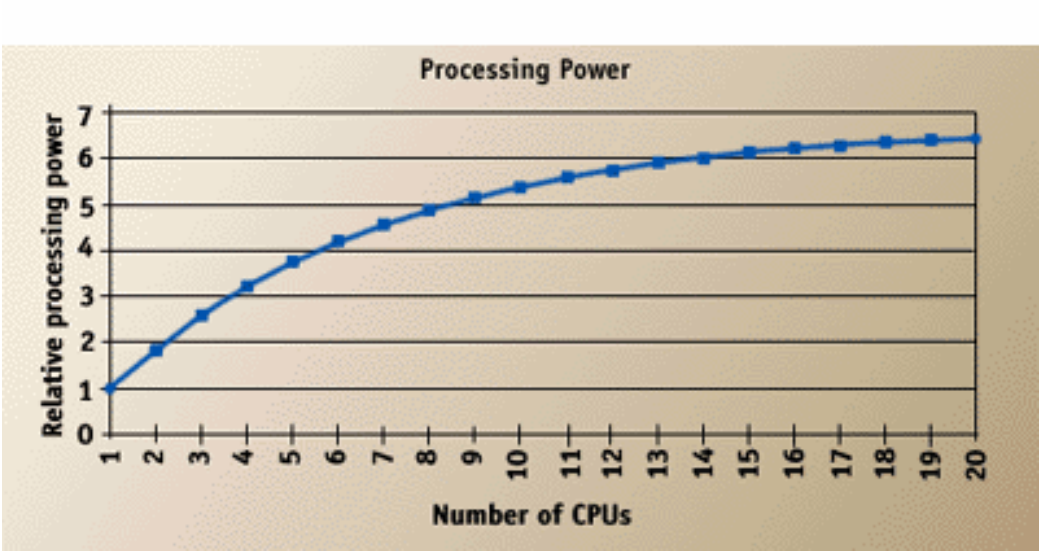

Figure 1: Multi processing effectiveness

New verification approach has come of age

Since conventional hierarchical, multi-processing model is proven non-effective for nanometer technologies, a new direction for physical verification come of age. The industry demands new solutions that are made of integrated methods. A new approach has come of age. This scalable approach can successfully handle large design size, nanometer challenges and rule deck complexity with greater efficiency, incorporating multi-processing and better database management. Newest physical verification concepts present new partitioning methods that remove multiprocessing limitations inherent to today's EDA tools. The development of advanced partitioning concepts has lead to high level of utilization across massively parallel computing resources. The new approach is based on compilers optimization to implement a combination of partitioning strategies that achieve an efficient usage of parallel processing resources. This approach enables the analysis of the design and rule deck during compile time to define and allocate processing tasks across available computing resources according to a variety of factors like priority, partition nature, etc'. This efficient task allocation approach optimizes the processing implementation to achieve performance and accuracy. This advanced partitioning technique is based on exclusive combination of rule deck terms, design characteristics and available computing resources to achieve an efficient resource leveling across large compute farms, eliminating long poles and speeding runtimes. Using this approach significantly increases overall system performance potentially utilizing unlimited amount of CPUs. Another new direction within recent verification approaches is to provide private high-level commands to handle specific complex checks. For example signal integrity issues such as reliability and density checks. These private high-level commands are replacing long sections of primitive commands that complicate rule decks authoring and causing processing delays. One can say that now we have a system that is construct of dedicated processing engines that analyzing each partition according to its characteristics. (Size, type of circuitry, Etc') There is no need to rewrite rule decks. The optimizing compiler automatically detects opportunities to allocate dedicated engines based on recognition of pre determined patterns in the input rule deck. In this way the tedious work of rewriting rule decks is avoided.

Another major advantage of this approach is accuracy improvement. Due to the fact that each engine is designed for a specific verification task, (according to partition characteristics), the end results is much higher accuracy level. One can say that each dedicated engine is an 'expert' in his field. It is designed to process a certain type of data rather than relying on the approximations inherent in a sequence of primitive verification operations. For example, in a reliability check mentioned above, tools using conventional primitive-level commands will not be able to detect situations that a specific engine would do. Combining private commands for dedicated processing engines is a strong solution for advance nanometer challenges. In this way newest, complex nanometer effects can be efficiently handle, fast!

These private commands implemented as dedicated processing engines take few lines, replacing potentially hundreds of lines in a typical rule deck, dramatically improving rule deck development and maintenance.

Data Management is essential

As the industry is moving forward with nanometer technologies new phenomenon are imposing more constraints on upstream design characteristics. One of the major issues is the data management. Industry's EDA verification tools are adopting an open architecture approaches such as OpenAccess for data management. The optimization of design data model is a key factor for overall system performance. Another essential factor is the ability to reduce the 'time per violation' factor which provides an important advantage in decreasing the number and magnitude of design iterations common in today's physical verification environments. OpenAccess-based physical verification tools write violations to the design database as they are discovered, permitting early identification of design errors. Therefore, if designers find serious violations as a verification run progresses, they can terminate the run and immediately begin working to fix these violations. This means major time saving during physical verification, achieving clean design with much less iterations.

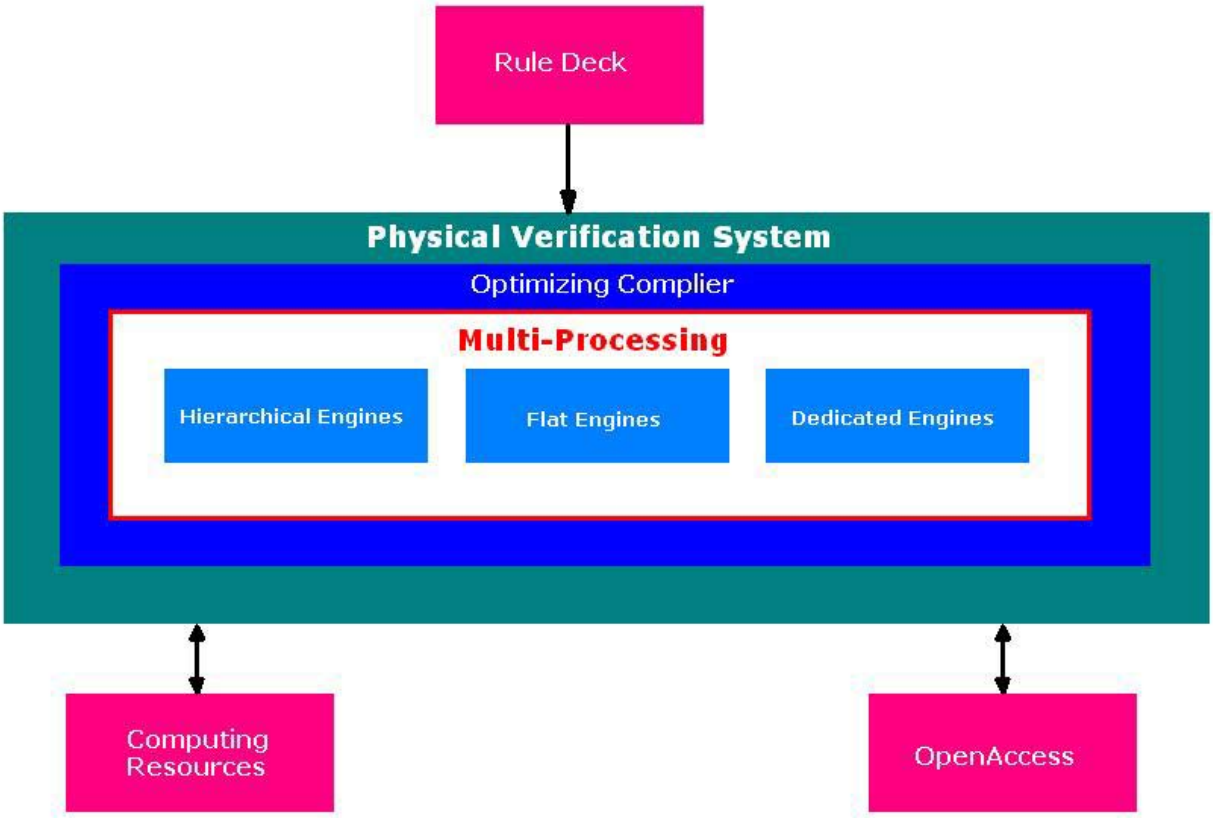

Figure 2: New Physical Verification Approach

The IC design world is in a constant race after nanometer technologies progress. With each new process designers face a whole new world of constraints and effects. This fact enforces EDA vendors to constantly develop new solutions and approaches for industry’s needs. As the process moves into 65 nm and below the current physical verification tools do not provide sufficient performance and accuracy. Consequently designs do not meet their tape-out schedules and furthermore, fail in basic functionality. A new approach has come of age. This combination of enhanced performance and open data architectures allows design teams to broaden the scope of physical verification checks to address complicate nanometer manufacturing issues that have a significant impact on yield. Designers no longer need to wait days for the minimum set of results that enables design signoff. Instead of waiting days for verification results that enable design signoff, the new approach in physical verification fully take advantage of the power of massively parallel processing environments and deliver an earlier, more accurate assessment of the design status and make a direct impact on the yield. The new, scalable approach to physical verification greatly enhances the designer's ability to deliver successful high-yielding designs that work on the first mask set, which is a significant payoff in the era of few thousands design rules, one billion transistors, and few millions dollars mask sets.

No Doubt, the industry’s emerging nanometer technologies virtually can not be fully utilized and exploit without new approach in physical verification.